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THE UNIVERSITY OF ALBERTA

A CMOS PIPELINE A/D CONVERTER

by

FREDERICK ROLAND SCHINDLER

A THESIS
SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH
IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE
OF MASTER OF SCIENCE

ELECTRICAL ENGINEERING

EDMONTON, ALBERTA
SPRING 1986

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"Everything should be made as simple as possible,
but not simpler."

Albert Einstein (1879-1955)

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research, for acceptance, a thesis entitled A CMOS PIPELINE A/D CONVERTER submitted by FREDERICK ROLAND SCHINDLER in partial fulfilment of the requirements for the degree of MASTER OF SCIENCE.

I. Filanovsky
Supervisor

J.d. Harrison

Keith A. Stromsmoe

Date APRIL 17, 1986

For my family, and in Opa's memory.

ABSTRACT

A new analog to digital pipelined algorithmic converter architecture is proposed and investigated. This device and the serial-flash converter in their cascade and pipeline forms are analyzed to determine how various error sources contribute to conversion errors. The analysis reveals the need for on chip error correction and various specialized circuits. Two unique circuits especially designed for the proposed analog to digital converter (ADC) include a high slew rate/low power consumption buffer amplifier, and an electronically calibrated precision gain circuit. The proposed ADC is designed to be fabricated using a digital CMOS process. No post process trimming is required if off chip voltage references are employed.

The proposed design has a flexible conversion characteristic which can be altered to provide nonlinear conversion. A trade-off can be made between the produced wordlength, and the die area used, or the maximum conversion rate possible. The digital wordlength of the proposed ADC chip can be easily increased without affecting the sample rate because of the converter's segmented structure and pipelining. That is, a second ADC may be connected to the first's expansion output to provide additional precision. This can continue to a maximum wordlength governed by stage error tolerances.

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Table of Contents

Chapter Page

1. INTRODUCTION TO A/D CONVERTERS 1

1.1 SAMPLING SYSTEMS 2

1.2 TECHNOLOGY 4

1.3 ADC BASICS 4

1.3.1 DIGITAL CODES 5

1.3.2 THE IDEAL ADC CHARACTERISTIC 7

1.4 NONLINEAR ADCS 10

1.5 STATE OF THE ART ADCS FOR MEDIUM TO HIGH SPEED CONVERSION 11

1.5.1 FLASH CONVERTERS 11

1.5.2 SUCCESSIVE APPROXIMATION CONVERTERS 13

1.5.3 CASCADED CONVERTERS 14

1.6 SOME ADC DESIGN CONSIDERATIONS 19

1.7 THESIS RESEARCH MOTIVATION AND GOALS 21

1.7.1 THE PROPOSED CONVERTER 23

2. ERROR ANALYSIS OF CASCADED AND PIPELINED CONVERTERS .24

2.1 ERRORS IN REAL ADCS 26

2.2 CONVERSION ERROR ANALYSIS 28

2.3 COMPARATOR ERROR ANALYSIS 32

2.4 SIMULATED STAGE ANALYSIS 34

2.5 ERROR ANALYSIS CONCLUSION 37

3. HIGH SLEW RATE/LOW POWER BUFFER AMPLIFIER DESIGN 39

3.1 FUNCTIONAL DESCRIPTION 39

3.2 BUFFER OPERATION IN DETAIL 43

3.2.1 OFFSET VOLTAGE REDUCTION 45

3.2.2 PRELIMINARY CONCLUSIONS 47

3.3 OFFSET VOLTAGE REDUCTION AND GAIN ENHANCEMENT ...49

3.4 BUFFER SUBCIRCUIT DESIGN 52

3.5 THEORETICAL CALCULATIONS 54

3.6 ENHANCED BUFFER AMPLIFIER CONCLUSIONS 57

3.7 SWITCHABLE OUTPUT BUFFER MODIFICATION 58

4. PRECISION GAIN AMPLIFIER DESIGN 60

4.1 SYSTEM STABILITY 64

4.2 ERROR SOURCES 65

4.3 PRECISION GAIN CIRCUIT IMPLEMENTATION 66

5. PRACTICAL REALIZATION OF THE ADC 68

5.1 THE SUBTRACTOR CIRCUIT 68

5.1.1 SUBTRACTOR ERROR SOURCES 70

5.2 THE INTERNAL ADC AND DAC 71

5.2.1 THE INTERNAL ADC'S COMPARATOR SELECTION ...72

5.2.2 THE ADC'S REFERENCE VOLTAGES 74

5.3 FULL STAGE ERROR CORRECTION PROCEDURES 75

5.4 NORMAL OPERATION 77

6. SIMULATIONS OF THE PROPOSED CONVERTER AND ITS FLEXIBILITY 82

6.1 SPICE SIMULATIONS 82

6.2 INPUT PARAMETER CALCULATIONS 83

6.3 MAXIMUM WORDLENGTH SIMULATION 88

6.4 THE PROPOSED CONVERTER'S FLEXIBILITY 101

7. CONCLUSION 105

7.1 FUTURE CONSIDERATIONS 107

7.2 THE PROPOSED ADC'S FEATURES AND POSSIBLE APPLICATIONS 109

REFERENCES 111

APPENDIX ONE 116

APPENDIX TWO 135

List of Tables

Table Page

3.1 Buffer amplifier parameters 59

5.1 Full stage process sequences 79

6.1 The proposed converter's internal error values 89

6.2 Parameters required for error value calculations 90

6.3 Maximum wordlength combinations 91

List of Figures

Figure Page

1.1 The ideal 3 bit ADC's characteristic 8

1.2 Flash converter architecture 12

1.3 Successive approximation converter architecture 12

1.4 Serial flash converter architecture 15

1.5 Algorithmic converter architecture 15

1.6 Pipelined algorithmic architecture of Muniappan's design 17

1.7 High-accuracy pipeline ADC configuration 17

2.1 Block diagram of the proposed ADC 25

2.2 Full stage of an algorithmic or series-flash converter with either cascade or pipeline architecture 25

2.3 Errors in nonideal ADCs (a) Offset; (b) Gain; (c) Linearity; (d) Differential nonlinearity 27

3.1 Simplified buffer circuit 40

3.2 Source follower configurations:(a) with common source and substrate connection;(b) with separate source and substrate connections. 44

3.3 Phase two buffer amplifier configuration 46

3.4 Simplified diagram of the buffer amplifier and its subcircuit 50

3.5 Unipolar transconductance amplifier 53

3.6 Enhanced buffer amplifier block diagram 55

4.1 Precision gain amplifier 61

5.1 Proposed full stage realization 69

5.2 Simple comparator with offset voltage reduction 73

6.1 Full stage of an algorithmic or series-flash converter with either cascade or pipeline architecture. 85

Figure Page

6.2 (a) Scatter plot of conversion error for an ideal conversion with N=8 s=r=2 and inc=4; (b) expanded view of one plotted quantization step 93

6.3 Scatter plot of conversion errors for the proposed ADC with N=8 and s=r=1 95

6.4 Scatter plot of conversion errors for the proposed ADC with N=8 and s=r=2 96

6.5 Scatter plot of conversion errors for the proposed ADC with N=8 and s=3 r=2 97

6.6 Scatter plot of conversion errors with ideal values of gain coefficients, and with N=8 s=r=2 99

6.7 Scatter plot of conversion errors with no offset voltages, and with N=8 s=r=2 100

LIST OF SYMBOLS

a	used in the error analysis, a=0 for the algorithmic converter, a=1 for the serial-flash converter
ADC	analog to digital converter
A/D	analog to digital
A_{INPUT}	an input stage gain
A_{OUT}	an output stage gain
A_{OBUF}	a buffer circuit gain without the subcircuit
A_{BUF}	a buffer circuit gain with the subcircuit
A_{OL}	an open loop gain
A_{MIN}	a minimum gain
A_{MAX}	a maximum gain
A_x	denotes a voltage gain, where x expands on its type or configuration
b	used in the error analysis, b=0 for cascade architecture, b=1 for pipelined architecture
BW	bandwidth
β	a feedback coefficient
BCD	binary coded decimal
b_j	bit j
C_x	capacitance referenced by its subscript x
CMOS	complementary metal oxide semiconductor
C_{ox}	the MOS gate capacitance per unit area
DAC	digital to analog converter
dB	decibel

δ	normalized error at the expansion output of an ADC
EPROM	electrically programmable read only memory
f_s	sample frequency
g_m	a MOSFET transconductance value
G_m	the transconductance of the buffer subcircuit
I_E	the full stage's integral linearity error
i	refers to the i^{th} stage
JFET	junction field effect transistor
K_S	the full stage's gain coefficient
K_R	the voltage reference's coefficient
LSB	least significant bit
λ	the subtractors gain coefficient
MOSFET	metal oxide semiconductor field effect transistor
M_x	denotes a MOSFET, where x may be a numerical value
n	number of full stages
NMOS	N-channel metal oxide semiconductor
NADC	nonlinear analog to digital converter
N	number of bits in the binary word
op-amp	operational amplifier
OP_x	denotes op-amp x, where x may be a numeric value
PMOS	P-channel metal oxide semiconductor
PCM	pulse coded modulation
r	number of bits produced by the partial stage

RMS	root of the mean squared
r_s	output resistance of the voltage source being discussed
R_k	denotes a resistance or resistor k, where k may be an alphanumeric value
R_X	the effective resistance between the drain and source of a MOSFET operating in its triode region
R_p	the effective resistance of R_C in parallel with R_X
S&H	sample and hold
S/N	signal to noise ratio
S	number of bits produced by a full stage
τ	maximum processing delay of a full stage
T_R	the number of times an input is recycled through a die area reduced ADC
V_t	threshold voltage of a MOSFET
V_{DD}	positive supply voltage
V_{SS}	negative supply voltage
V_α	ideal V_{GS} of the simplified buffer circuit's NMOS devices conducting current I
V_x	denotes a voltage x, where x may be an alphanumeric value
V_{SE}	the full stage's voltage reference independent, offset voltage
V_{SEZ}	the full stage's voltage reference independent offset voltage for the minimum input value

V_{SI}	the full stage's DAC voltage and voltage reference dependent offset voltages
V_{EXP}	the expansion output voltage
V_{EXPI}	the ideal expansion output voltage
V_{IN}	an input voltage
V_D	is a correction factor used in the error analysis when the internal flash converter produces all zeros
V_d	the voltage to be subtracted using the subtractor
V_{gs}	the gate source voltage drop for the specified transistor; capital subscripts imply DC, while lower case subscripts imply AC
V_O	an output voltage, also indicated as V_{OUT}
V_{ros}	the offset voltage, of the stage offset voltage measuring circuit
V_{CO}	a comparator offset voltage
V_{NI}	comparator voltage error tolerance at stage i
V_{NP}	is V_{NI} calculated for the partial stage
V_{REF}	system voltage reference
word	the digital output/input of an ADC/DAC
x(nT)	the analog equivalent of a digital representation at time nT
Z_o	an output impedance
2^{-w}	weighting factor
2^{-N}	normalized LSB

1. INTRODUCTION TO A/D CONVERTERS

Analog to digital converters (ADC) are devices which translate an analog signal into a digital representation. That is, a voltage or current (the analog signal) is converted to a number (the digital value). The analog signal is usually produced by another device known as a transducer. This element transforms energy into the electrical quantities required for the ADC. For example a microphone is a transducer that transforms the vibrations of air molecules due to sound into electrical power.

It is desirable to represent a voltage or current digitally, because this improves the storage and manipulation ability as well as the integrity of the converted information. This becomes possible because the numbers are represented in binary as ones (1) and zeros (0). Therefore, only two discrete electrical quantities are required in a digital system, while an analog system covers a considerably broader range of values. The digital representation of a quantity preserves the signal to noise (S/N) ratio better in comparison to an analog representation of the same quantity. By virtue of the binary form, a larger amount of noise can be tolerated before an incorrect value is produced. Due to poor component tolerances and noise, analog systems are less reliable than digital systems [ROTH,1979]. As a result of the many useful properties of digitized analog signals, ADCs are used in many areas. These include: audio, video, control systems and instrumentation.

Once the digital information has been processed it can be transformed back to an analog quantity (voltage or current) by a digital to analog converter (DAC).

1.1 SAMPLING SYSTEMS

Analog to digital converters can be put into separate groups by looking at the rate at which they can convert analog quantities to their digital representation [SOCLOFF,1985]. This is an important factor because the conversion rate will limit the number of applications a particular converter can be used for. Different applications have varying bandwidth (BW) requirements, and different frequency ranges of operation. For example an audio application typically requires frequencies ranging from 20 Hz to 20 KHz, while an instrumentation application that measures d.c. voltages has an operating range around 0 Hz.

The conversion rate is determined by the highest frequency component that must be digitized. This conversion rate is also known as the sample frequency (f_s). It is determined by the Nyquist criterion which indicates that the sample rate must be greater than twice the highest frequency component [STERNS,1983]. When this criterion is met, all the information conveyed in the analog signal is available in the ideally sampled version.

An approximation to ideal sampling is possible. When low speed conversion is required a fast ADC may be used without any additional hardware [GREBENE,1984;CLAYTON,1984].

More often though, a sample and hold circuit (S&H) is used because it permits data conversion of higher frequencies. The S&H circuit has two modes of operation. It first samples an analog input (sample mode) and tracks its value until the hold mode is initiated. In the hold mode the input value just prior to the mode is held constant at the S&H's output. Therefore, analog to digital conversion is carried out while the S&H circuit is in its hold mode.

When the frequency spectrum of the resulting waveform approximation is analyzed, it can be seen that some low pass filtering has occurred [STERNS,1983]. In addition to this, amplitude reduction of the original spectrum shifted about integer multiples of the sample frequency has occurred. The envelope of this filtered characteristic is well known and can be mathematically described [STERNS,1983]. Therefore, manipulation of the original spectrum is possible.

If the sample frequency is below the required value, or frequencies higher than are permitted are sampled an overlap of the shifted spectra occurs, which is known as *aliasing*. This aliasing would corrupt the original spectrum. Therefore, frequencies outside the desired BW can be considered as noise. For this reason an antialiasing low pass filter is usually used to limit the input spectrum prior to the sampling. Moreover, sample frequencies of an order of magnitude above the required Nyquist maximum are used so that the antialiasing filter's roll-off characteristic does not affect the desired spectrum. A lower order antialiasing filter may then be adequate.

1.2 TECHNOLOGY

A number of semiconductor technologies have been used to produce ADCs, which include: bipolar, NMOS, PMOS and CMOS. Only two of the technologies are being used extensively at present, bipolar and CMOS. Bipolar technology was the first used, and still provides the fastest conversion rates. The latest process used to produce converters is CMOS, because both analog (the converter) and high density digital logic circuits can coexist on the same chip. Furthermore, CMOS technology lends itself better to the sampling process employed in analog to digital conversion. That is, capacitors and analog switches are more readily formed with better tolerances and qualities than in the other processes [GRAY,1984]. PMOS and NMOS are rapidly disappearing from the conversion design area because both processes lack complementary devices. PMOS has the additional burden of being slow because holes are used as a transportation mechanism whereas NMOS employs electrons for transport.

1.3 ADC BASICS

Features common to all converters will be covered in this section. The concepts covered include: digital codes, the ideal ADC characteristic and basic ideas on nonlinear conversion.

1.3.1 DIGITAL CODES

The majority of the ADCs use binary to represent data but there are several different encoding schemes used [ROTH,1979;CLAYTON,1984]. The most frequently used are binary, and Gray code. Binary is a weighted code while Gray code is not. A weighted code places a fixed value for every bit position in the digital output. Gray code does not do this, but it has the advantage that adjacent digital numbers differ by only a single bit. This feature tends to lower processing transients and delays.

Most of the ADCs used produce binary, as will the proposed ADC, hence this representation will be discussed more completely than Gray code. A digital representation of a *unipolar* analog signal (single polarity inputs only) in binary, sampled at time nT is given by:

$$x(nT) = V_{REF}[\ b_{N-1}2^{-1} + b_{N-2}2^{-2} + \cdots + b_0 2^{-N}\ ] \tag{1.1}$$

where V_{REF} is the *reference voltage* and $b_j 2^{-w}$ is the bit (b_j) and weighting factor (2^{-w}) to be evaluated. The value N is the number of bits used in the digital representation, and it is also known as the converter's *wordlength*. As a consequence of this representation, a quantization error of at least 1/2 a least significant bit (LSB, $V_{REF}2^{-N} = 1$ LSB) can result. This occurs because the digital output remains constant for 1 LSB steps over the input range.

When using binary with a word size of N bits, there are 2^N possible numbers. The first combination where all bits are zero is considered to be the numerical zero as well. Therefore, since there are only 2^N-1 combinations after zero the maximum digital output (all bits are one) corresponds to an analog value of 1 LSB less than V_{REF}. Even though this is the case, it is common practice to specify the analog input range of an ADC as extending to V_{REF}.

Analog to digital converters can be made to digitize analog signals of both polarities. This is known as *bipolar* operation. The simplest way to accomplish bipolar operation is to add $V_{REF}/2$ to the input of a unipolar ADC prior to digitization. Therefore, the new input range now extends from $-V_{REF}/2$ to $V_{REF}/2$ because the resulting sum goes from 0 to V_{REF} which is within the limits of the unipolar ADC. In some conversion techniques it is possible to either invert the positive reference or provide two references of opposite polarity. In either case the reference used depends on the sign of the input, but the range may now extend from $-V_{REF}$ to V_{REF}.

For bipolar operation the input range is not identical to the actual limits available. The maximum digital output ideally is 1.5 LSB lower than the specified limit while the lower limit is given correctly. It is also possible for the exact opposite, depending on the analog to digital conversion method chosen [GORDON,1978]. This will produce a maximum quantization error of 1 LSB at one of the extremes.

Several digital encoding schemes are used to represent bipolar numbers but *two's complement* notation is the most frequently used. This counting scheme is well explained in most basic digital electronic textbooks [ROTH,1979]. Some methods obtain the two's complement number directly while others must use a logic network to transform the direct result into this notation.

The first method of bipolar conversion discussed above results in offset binary numbers. That is, all digital representations are positive but require the arithmetic subtraction of the digital code for the $V_{REF}/2$ quantization level to result in a correct two's complement binary form. The two's complement notation is more easily obtained by complementing the MSB of the offset binary word.

1.3.2 THE IDEAL ADC CHARACTERISTIC

Concepts to be outlined below are illustrated in figure 1.1 . The graph represents an ideal 3 bit ADC's conversion characteristic. To produce this representation all ADC effectively offset the input by adding the electrical equivalent of 1/2 LSB to the input prior to conversion. This addition is performed so that the absolute error is within 1/2 LSB about the exact value, rather than a single polarity error of as much as 1 LSB. The sum is then compared in some fashion to all the possible threshold voltages. *Threshold voltages* occur at points where the digital words just change. The midpoint in between two

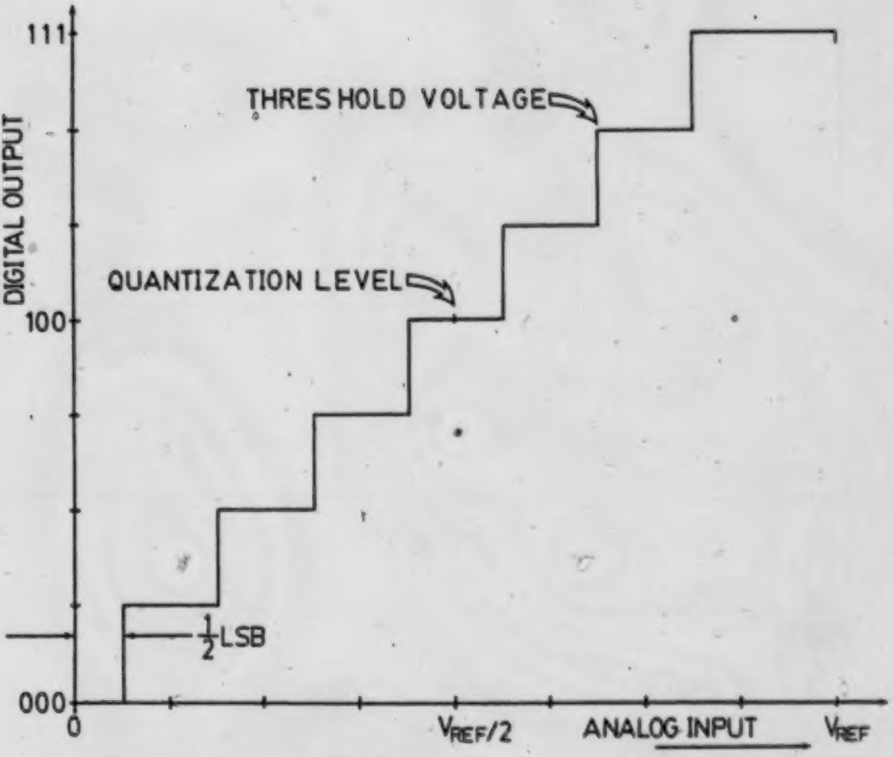


Figure 1.1 The ideal 3 bit ADC's characteristic

adjacent threshold levels is known as the *quantization level*. At this point, for an ideal converter the digital representation exactly matches the value of the analog input.

As previously mentioned, digital representations of numbers can have high S/N ratios that do not deteriorate with digital processing as much as the analog value would in an equivalent analog system. Once a quantity has been digitized, the S/N ratio of the system is determined by the wordlength's size. This measure is usually specified in decibels (dB). Assuming a sinusoidal input which extends over the entire range of the ADC and a triangular error voltage, an approximation to the highest achievable S/N ratio is given by [ANALOG DEVICES,1986]:

$$(S/N)= 6.02N + 1.8 \text{ dB} \qquad (1.2)$$

The S/N ratio of an ADC when the maximum quantization level is converted would have the term 10.8 added to the variable value instead of 1.8 in formula (1.2) [LORIFERNE,1982]. This formula less the constant indicates the dynamic range of the converter [GREBENE,1984]. The S/N specification deteriorates as the input amplitude decreases. To overcome the deterioration of this specification, nonlinear (also referred to as nonuniformed) ADCs can be used.

1.4 NONLINEAR ADCS

In many applications employing transducers the generated analog signal may not be linearly related to the quantity being transduced. This problem can be reduced by using a nonlinear ADC (NADC). A NADC with the correct transfer characteristic can provide a linear relationship between the transduced quantity and the digital word. The linearization process could also be accomplished after the analog signal has been digitized linearly, but the dynamic range is reduced by this method or precision is wasted in some regions of the transducer characteristic. Nonlinear converters permit the precision to be placed only where it is required.

Nonlinear ADCs are also used for pulse-coded-modulation (PCM) voice encoding of telephone conversations [GREBENE,1984;TSIVIDIS,1979]. This nonlinear conversion is also called *companding*, which indicates compression/expansion is being performed. Companding in telephony is performed on standard voice channels using the *μ-255 law* [GREBENE,1984]. At the receiving end of the system decoding is performed using a companding DAC. The reason this procedure is used is that the S/N ratio remains essentially constant over most of the input range. This occurs because the precision increases as the signal level decreases. Hence the ratio of the maximum error to the signal at almost any point in the transfer characteristic is approximately constant [LORIFERNE,1982].

1.5 STATE OF THE ART ADCS FOR MEDIUM TO HIGH SPEED CONVERSION

This research is primarily concerned with medium to high speed converters ($20KHz \leq f_s \leq 20MHz$) in their integrated form, hence only conversion methods in these categories will be briefly discussed. Moreover, only voltages will be used as analog inputs when describing the ADCs, but a current equivalent may also exist. The methods detailed below are illustrated for unipolar operation, but may be modified as described previously to result in bipolar operation.

1.5.1 FLASH CONVERTERS

The fastest known ADC is referred to as the flash or parallel converter (figure 1.2). In this method the voltage to be digitized is applied to a comparator network. Each comparator used has a unique fraction of the reference voltage associated with it. The comparators produce a binary result, which is dependent on whether the input voltage is greater than or less than the portion of the reference used in the comparison. Connected to the comparator's outputs is a logic network which produces the digitized representation. This method requires a large amount of die area, because 2^N-1 comparators are required for an N bit word. Furthermore, if resistors are used to produce the required fractions of V_{REF} a total of 2^N precise resistors are also required.

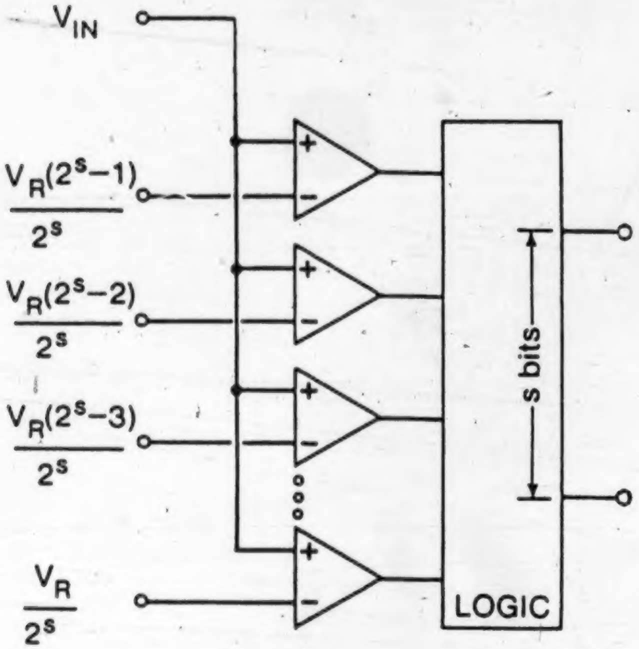

V_IN
V_R(2^s−1)/2^s
V_R(2^s−2)/2^s
V_R(2^s−3)/2^s
V_R/2^s
+
−
s bits
LOGIC

Figure 1.2 Flash converter architecture

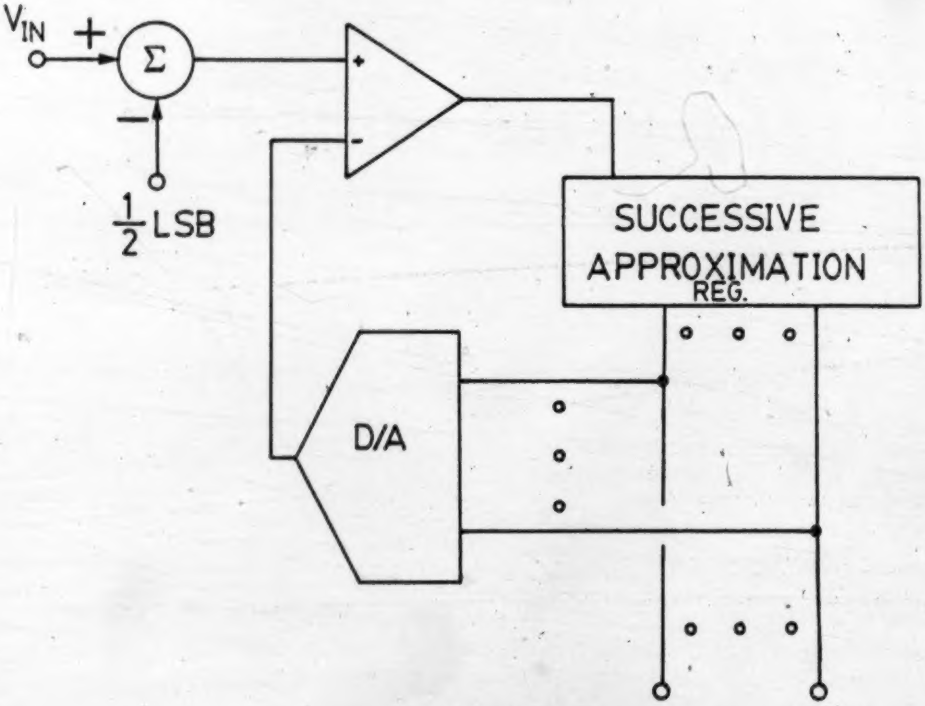

V_IN
+
−
Σ
1/2 LSB
SUCCESSIVE APPROXIMATION REG.
D/A

Figure 1.3 Successive approximation converter architecture

An additional drawback to this method is that there is a limit on the maximum wordlength achievable [GREBENE,1984].

1.5.2 SUCCESSIVE APPROXIMATION CONVERTERS

Probably the most commonly used converter is the successive approximation converter (figure 1.3). It operates at a medium sample rate with a considerably lower component count than the flash converter. Only a single comparator is implemented. Here the input with the 1/2 LSB subtracted from it is sucessively compared to the output of a DAC. The digital inputs of the DAC are connected to a digital logic circuit known as the *successive approximation register*. This device varies the digital input of the DAC starting at one LSB below the mid-range quantization level. Therefore the most significant bit (MSB) is presently reset while all the following bits are set. Depending on the comparator's value the MSB may be set, if the input is greater than the present comparison voltage or left reset for the opposite case. Once this has been completed, the MSB remains at its determined value and the process resumes at the next lower valued bit. That is, the next bit is reset and then determined via the comparison procedure. This continues until the desired wordlength has been established. Furthermore, a wordlength greater than is possible in the flash conversion method is achievable.

1.5.3 CASCADED CONVERTERS

The next methods are all derived from the conversion schemes detailed above. Flash converters of a given size may be used to form larger wordlengths. In this conversion method an input signal has its most significant s bits determined first by an s bit flash converter. This digital value is then fed into a DAC which produces a signal equivalent to the s determined bits. Following this the DAC's output voltage is subtracted from the original input. The difference signal is then digitized using a second flash converter that produces r additional bits. Therefore, a total of $s+r$ bits precision results. To produce the correct weighting factors the first ADC uses V_{REF} as a reference while the second has its reference voltage set at $V_{REF}/2^s$ (figure 1.4). Alternatively the same reference voltage could be used in both stages but a gain of 2^s would be required between the output of the first and the input of the second stage (figure 1.5). These conversion methods provide larger wordlengths with a lower component count than a purely flash conversion approach at the expense of lowering the sample rate [GREBENE,1984]. These methods can go beyond two stages but internal errors introduced place a limit on the number of stages and/or bits possible (see chapter two). The first method that employs the flash converter without gain is usually referred to as: a *series-flash* or *series-parallel* converter. When the gain is used, the conversion method is usually called: *algorithmic*, *two-step* or *series-parallel* as

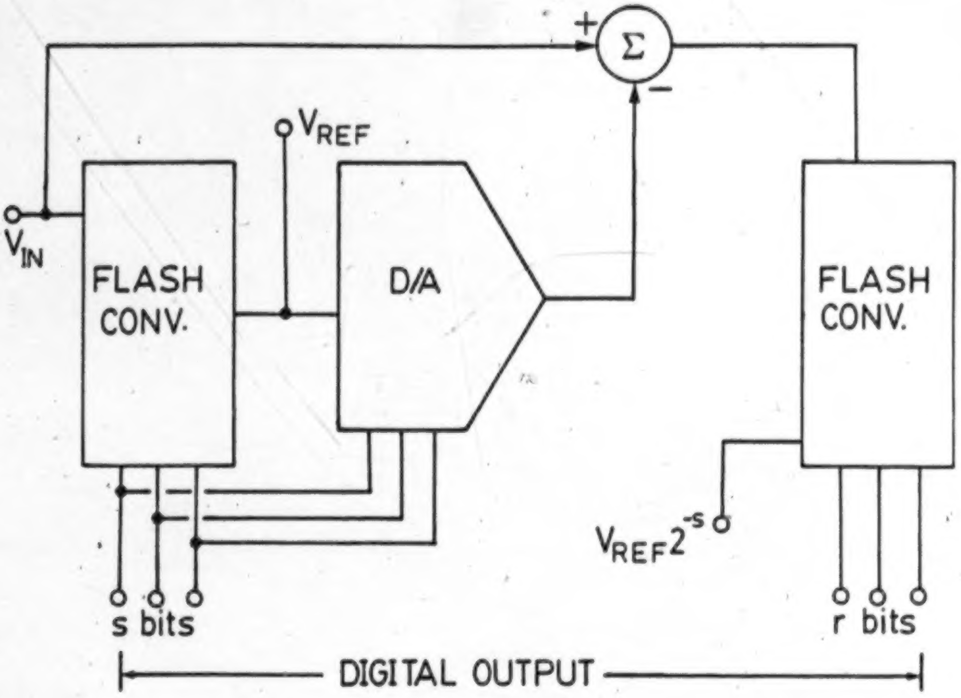

+
Σ
−
V_{REF}
V_{IN}
FLASH CONV.
D/A
FLASH CONV.
$V_{REF}2^{-s}$
s bits
r bits
DIGITAL OUTPUT

Figure 1.4 Serial flash converter architecture

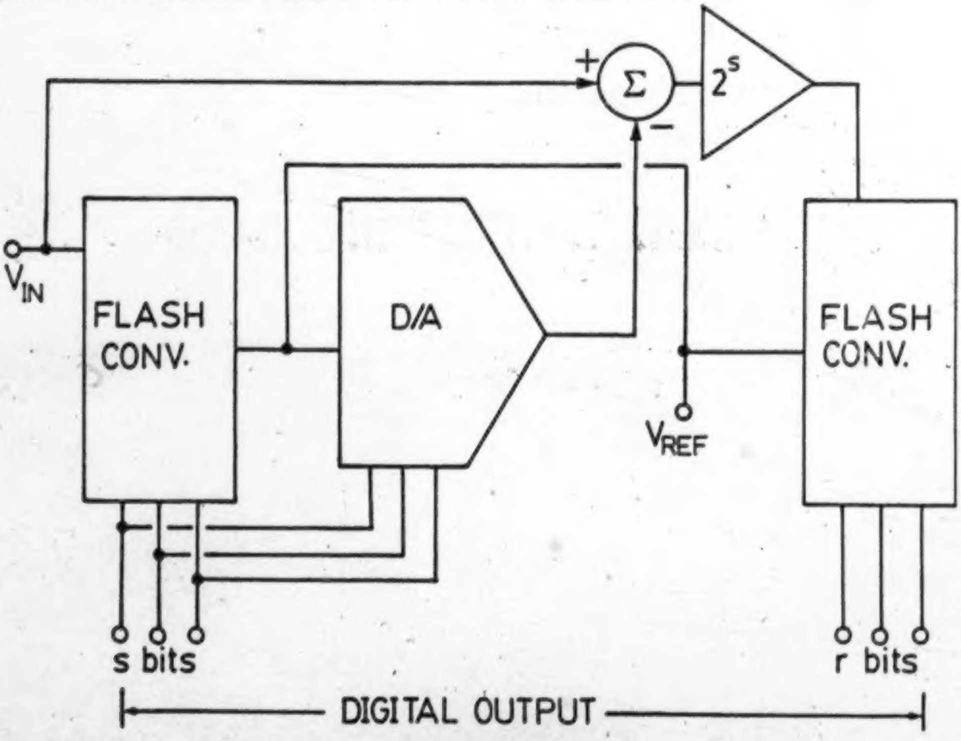

+
Σ
−
2^s
V_{IN}
FLASH CONV.
D/A
V_{REF}
FLASH CONV.
s bits
r bits
DIGITAL OUTPUT

Figure 1.5 Algorithmic converter architecture

well. The word serial is also used in place of series by some authors for the above names.

A modified algorithmic converter, which determines only one bit per stage with no restriction on the number of stages was proposed by K. Muniappan [MUNIAPPAN,1981]. The proposed converter combined research on series-parallel converters [NINOMIYA,1980;WOODS,1980] with basic pipelining steps in digital signal processors [ASHOURI,1977] [GORGINSKY,1970] to produce a method of pipelining ADCs. This is accomplished by inserting both analog and digital delays. Figure 1.6 presents a three bit ADC block diagram based on Muniappan's architecture.

Analog delays of τ seconds are used between one stage's output and the next's input. Digital delays of $\tau(N+1-I)$ seconds are used, where I is the stage count (the input is the first stage) and τ is the maximum processing delay of a stage. These delays allow each stage to work on a bit from separate samples concurrently. To illustrate this point, a sample entering the ADC will be partially followed through it. After τ seconds the MSB has been determined and the processed input is passed to the next stage so that the second bit may be determined. As the transfer from the first stage occurs a new sample enters the stage. Therefore, at this time two samples are being processed. After the elapse of another τ seconds the MSB of the second sample and the second bit of the first sample are then shifted down one stage as a third enters the converter. Hence after $N\tau$

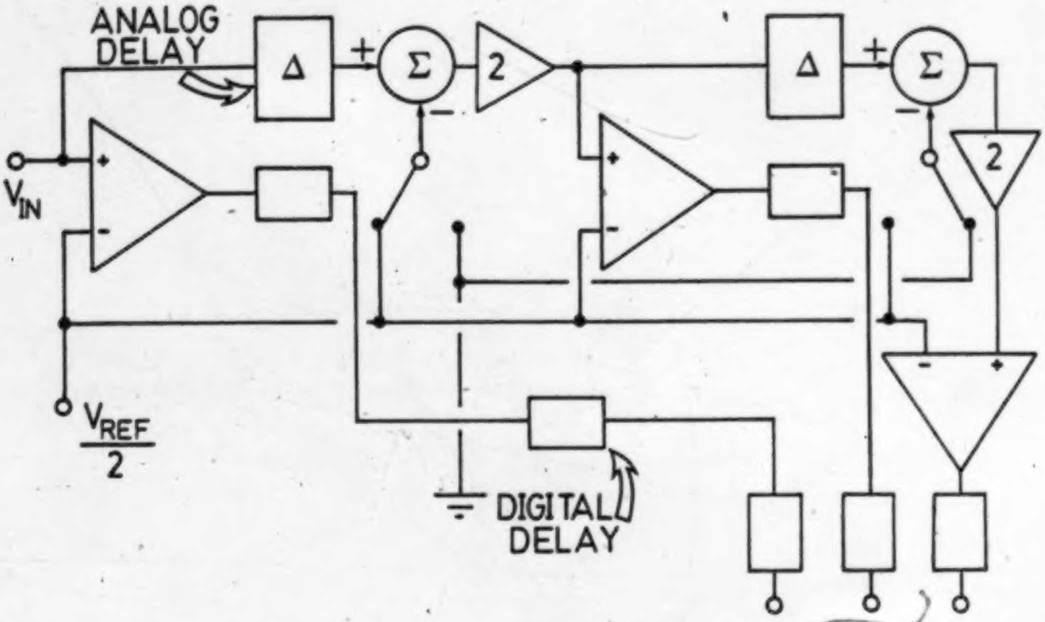

ANALOG DELAY
Δ
+
Σ
-
2
Δ
+
Σ
-
2
V_{IN}
$\frac{V_{REF}}{2}$
DIGITAL DELAY

Figure 1.6 Pipelined algorithmic architecture of Muniappan's design

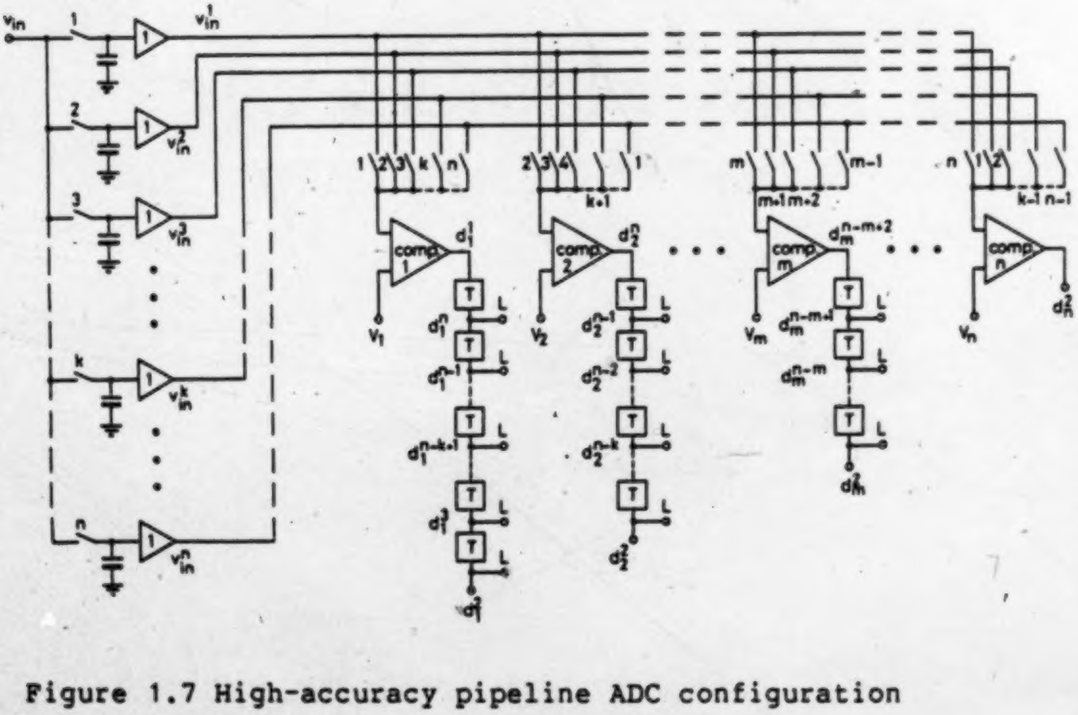

v_{in}
v_{in}^1
v_{in}^2
v_{in}^3
v_{in}^k
v_{in}^n
comp 1
comp 2
comp m
comp n
V_1
V_2
V_m
V_n
T
L
d_1^1
d_2^n
d_m^{n-m+2}
d_n^2
m+1 m+2
k+1
k-1 n-1
m-1

Figure 1.7 High-accuracy pipeline ADC configuration

seconds, the time it takes the first sample to be digitized, a valid sample reoccurs every τ seconds. If a pipelined architecture is used the sample period is N times shorter than in a standard algorithmic approach. The initial delay that results because of pipelining can be tolerated in most applications.

Another pipeline architecture (figure 1.7), proposed by G.C. Temes [TEMES,1985], also combines the useful properties of the flash and successive approximation converters. It was referred to as a "high-accuracy pipeline A/D converter configuration" because it does not corrupt the sampled input as it is processed. For an N bit converter, N stages and S&H amplifiers are required. The first stage compares the first sample to $V_{REF}/2$ to form the MSB. Then the second bit is determined in the next stage using another comparator. This comparator compares the original sample to the second stage's comparison voltage. The comparison voltage used is formed by adding the previously determined bit's value to the value of the second bit's position. As the second bit of the first sample is being determined, the second sample is having its MSB evaluated in the first stage. This process continues until the required precision is obtained. If each stage has a maximum delay of τ, the first valid result is made available in $N\tau$ seconds while the following digital outputs occur every τ seconds as was the case in the previous pipeline converter.

1.6 SOME ADC DESIGN CONSIDERATIONS

At present the digital die area and processing steps take precedence over the analog circuitry. This makes it difficult to provide both accurate ADCs and DACs. To circumvent this problem several on chip error correction schemes have been implemented. Some of the on chip error correcting techniques used on converters similar to the one to be proposed will be briefly detailed.

A ratio-independent algorithmic analog to digital conversion technique using CMOS technology has been reported by Li et al. [LI,1984]. An error correction method is used to reduce errors that occur when a gain of two is realized. Using a switch capacitor integrator, an output of n times the ratio of the input to feedback capacitors multiplied by the input voltage is formed. Then the capacitors used are electronically exchanged to produce an output voltage of n times the input voltage. The error due to capacitor mismatching is cancelled because in the final result their values do not appear.

Another technique reported by Lee et al. [LEE,1984] is also used to reduce capacitor matching errors. This method was employed for a charge redistribution successive approximation converter. In this technique, matching errors are determined by splitting the reference voltage between a discharged capacitor in series with a reverse reference voltage charged capacitor. If the capacitors are matched no voltage should be present across the previously reverse charged capacitor. This is possible because the charge necessary to reduce the previously reverse reference charged capacitor to zero is identical to the amount required to produce the reference voltage across the previously discharged capacitor. The voltage that does occur is an indication of the mismatch. With this information an error term is stored on chip in RAM. Therefore, during normal operation the errors measured can be compensated for.

A similar method was previously used by Boyacigiller et al. of Intersil Inc. [BOYACIGILLER,1981]. This error correction method was also used with a successive approximation converter, but with one that uses the technique outlined in this chapter. Here the calibration procedure (error correction) is performed only once. It begins by using a known input reference to produce a digital representation which is digitally modified until the correct value results. The term used to produce the required digital output is stored on an internal EPROM. This process is performed for all the quantization levels.

When portable equipment is used another factor to be considered is power consumption. This demand can conflict with the speed requirement, because bias currents of the circuits in the ADC must be increased to allow for higher speed operation [GRAY,1984]. The course of action taken by the digital designers is to use CMOS. This does not usually reduce the analog circuit's power requirements but can actually increase the power when compared to a comparable bipolar design [GRAY,1984;GREBENE,1984].

Another deciding factor in choosing an analog to digital conversion method, is the flexibility of the design. That is, once a considerable amount of effort has been expended on a converter design, can the converter be easily modified to suit new requirements? For example a good design permits as many of the following points as is possible.

1. A linear converter can be made to have a nonlinear characteristic.
2. There can be a speed versus wordlength trade-off.
3. There can be a power versus speed trade-off.

1.7 THESIS RESEARCH MOTIVATION AND GOALS

With the steadily increasing demand for microprocessor controlled products there has been a need for on chip microprocessors and analog conversion circuitry. This leads to lower costs and more reliable devices. Some of the products included in this list are: automobile measurement and control systems, high fidelity audio and television systems, portable medical equipment and much more.

Recent ADC designs incorporate new technologies, such as CMOS, to reduce the die area and power consumed by the conversion circuitry [DINGWALL,1979]. However these designs use well established conversion methods such as flash and successive approximation converters. Although these designs provide benefits due to the technology change, some of the less desirable features of the conversion scheme are also carried over. Problems such as limited wordlength, slow conversion, and high device tolerances are still present. Some designers choose to use both new technologies and architectures not possible in other technologies [FOTOUHI,1979;McCREARY,1975;SUAREZ,1975]. These designs however produce converters in the lower end of the medium conversion speed scale (f_s < 100 KHz). For this reason new avenues should be explored in order to arrive at a faster converter, formed using both new technology improvements and new or not fully investigated ADC technique.

An ADC which could overcome the majority of the design hindrances previously outlined, and still provide medium to high speed conversion would be very useful. With this as the initial goal, a suitable architecture was sought.

1.7.1 THE PROPOSED CONVERTER

After a search through the various conversion techniques that fit into the specified guidelines, the paper previously discussed by K. Muniappan [MUNIAPPAN,1981] set this research into motion. With this concept as a base, a more thorough investigation was in order before such a device could be fabricated. This research detailed herein is intended to provide the following, in this respect.

1. Expand the analysis to allow for variable wordlength stages.
2. Begin some basic error analysis of such a converter.
3. Begin circuit design of various specialized stage parts.
4. Provide some suggestions so that continuing research can lead to a fabricated design.

2. ERROR ANALYSIS OF CASCADED AND PIPELINED CONVERTERS

An important part of designing a circuit is deciding where errors accumulate and bottlenecks occur. In order to design the proposed ADC the basic pipelined algorithmic structure of Muniappan was transformed into a schematic. At this point various error sources such as: op-amp offset voltages, switch charge injection, subtractor error, and gain errors were revealed [SCHINDLER,1984]. Steps were then taken to remove the errors encountered. Although this procedure encompassed a fair bit of work the specifics are not important, but the error sources and error correction information obtained is. It is with this information that the initial steps of the error analysis were undertaken.

The following information is intended to provide an approximate starting point in determining the maximum permissible wordlength [SCHINDLER,1985]. A worst case error analysis approach was taken. This leads to some unlikely possibilities such as all op-amps having the worst case offset voltage, or all errors that can accumulate accumulating without any cancellation. The block diagram of the converter being considered is shown in figure 2.1. It illustrates a general structure consisting of $n=(N-r)/s$ full stages, each providing s bits of information, and a single partial stage which produces r bits.

To provide error analysis information on both algorithmic and series-flash converters the block diagram of a full stage, shown in figure 2.2, is used. Both converters

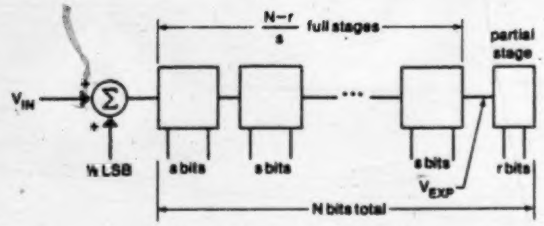
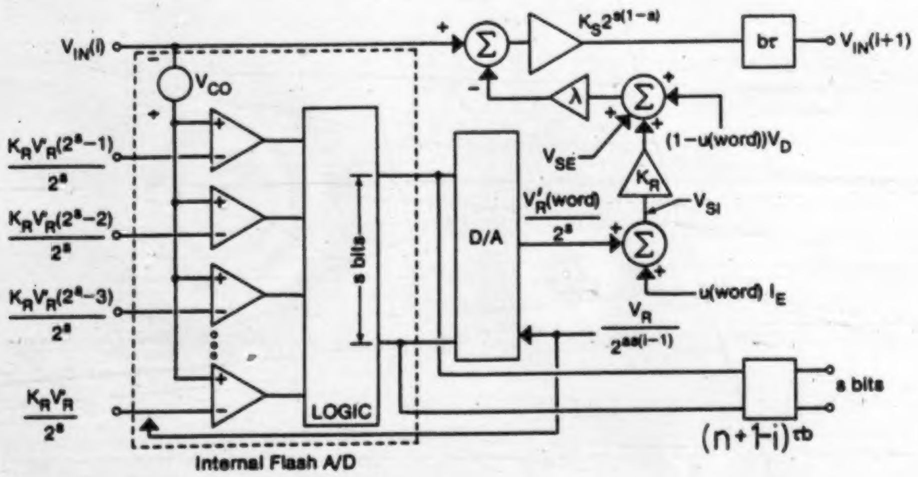

$\frac{N-r}{s}$ full stages
partial stage
V_{IN}
+
+
Σ
½ LSB
s bits
s bits
s bits
r bits
V_{EXP}
N bits total

Figure 2.1 Block diagram of the proposed ADC


$V_{IN}(i)$
V_{CO}
$\frac{K_R V_R(2^s-1)}{2^s}$
$\frac{K_R V_R(2^s-2)}{2^s}$
$\frac{K_R V_R(2^s-3)}{2^s}$
$\frac{K_R V_R}{2^s}$
LOGIC
s bits
Internal Flash A/D
D/A
$\frac{V_R'(\text{word})}{2^s}$
$\frac{V_R}{2^{as(i-1)}}$
$K_S 2^{s(1-a)}$
bτ
$V_{IN}(i+1)$
λ
V_{SE}
$(1-u(\text{word}))V_D$
K_R
V_{SI}
$u(\text{word})\ I_E$
s bits
$(n+1-i)^{\text{tb}}$

a=1 -flash converter   b=1 -pipelined version
a=0 -algorithmic converter   b=0 -cascade version

u(x)=0 ; x=0 $V_R' = V_R/2^{as(i-1)}$
u(x)=1 ; x>0

V_R - the converter's reference voltage
V_{CO} - maximum comparator offset error
K_S - stage's gain coefficient ($K_S=1$)
V_{SE} - various internal error offset voltages
V_D - used to change the error when the digital output of the stage is zero
V_{SI} - the ideal D/A output summed with V_R dependent quantities
I_E - integral linearity error of the D/A
word- the numerical value of the D/A's output ($0 \le \text{word} \le 2^s-1$)
K_R - stage's reference voltage coefficient ($K_R=1$)
λ - subtractor's gain coefficient ($\lambda=1$)

Figure 2.2 Full stage of an algorithmic or series-flash converter with either cascade or pipeline architecture

are realized by using the appropriate value of a (a=0 for the algorithmic converter, a=1 for the series-flash converter). Furthermore, a standard (cascade) architecture (b=0) or pipelined version (b=1) is determined by parameter b. The partial stage in either case, only consists of an r bit flash converter.

For this analysis it is assumed that the first stage's input has the voltage equivalent of 1/2 LSB added to it prior to the conversion. This addition is usually not done in series-flash conversion, rather each reference voltage would be effectively offset by 1/2 LSB. Both procedures produce the same result, since voltage differences are only significant to the comparators used for the conversion procedure. Therefore, valid information for either method will be obtained if this assumption is made.

2.1 ERRORS IN REAL ADCS

Before beginning the error analysis, a brief discussion of errors that occur in real ADCs will be covered. Four errors which most designers and manufacturers include on the finished device specification sheet are: offset, gain, linearity, and differential nonlinearity [HARRIS,1984]. These characteristics are shown separately and independently in figure 2.3, but they are all usually present to some degree in a real converter.

Most of the errors illustrated are intuitively understood. Therefore, only subtleties will require a

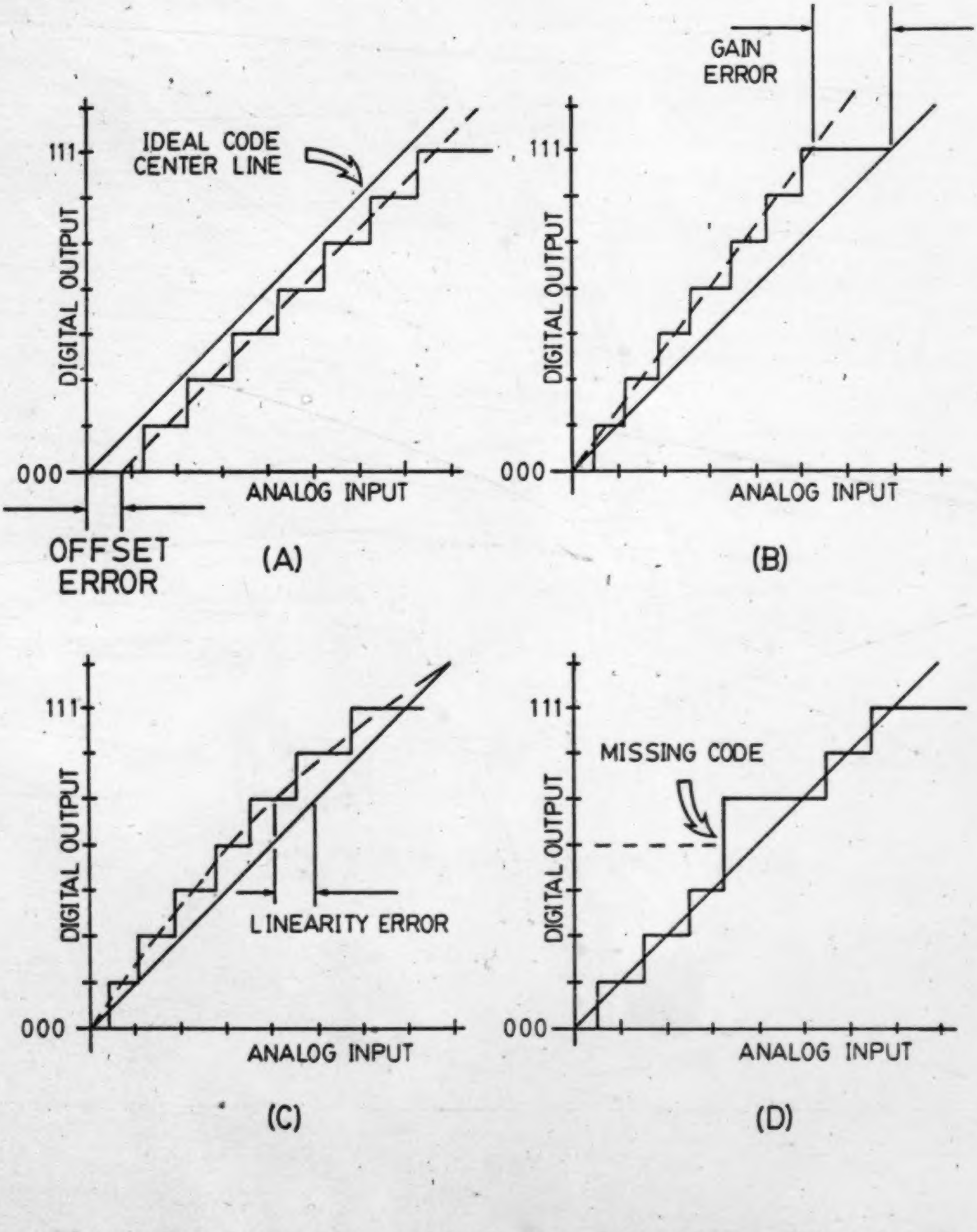

IDEAL CODE CENTER LINE
111
000
DIGITAL OUTPUT
ANALOG INPUT
OFFSET ERROR
(A)
GAIN ERROR
111
000
DIGITAL OUTPUT
ANALOG INPUT
(B)
111
000
DIGITAL OUTPUT
LINEARITY ERROR
ANALOG INPUT
(C)
111
000
MISSING CODE
DIGITAL OUTPUT
ANALOG INPUT
(D)

Figure 2.3 Errors in nonideal ADCs (a) Offset; (b) Gain; (c) Linearity; (d) Differential nonlinearity

further explanation. *Linearity errors* in this thesis will be expressed as some portion of a LSB which indicates the difference between the actual quantization point and the ideal characteristic's quantization point. The term *integral nonlinearity error* is used by some authors to represent the maximum value of the linearity error. *Differential nonlinearity* indicates the deviation the actual ADC's step size differs from the ideal 1 LSB width. If this error exceeds ±1/2 LSB a missing code can result. That is, at least one of the digital representations of an analog input is not obtainable.

2.2 CONVERSION ERROR ANALYSIS

In this analysis, the region where the worst case error occurs will attempt to be calculated as a function of the converter's parameters. To allow for a variety of stage variations, the stage's parameters are formed into three general groups. These groups include, gain errors (K_S,K_R,λ), offset voltages (V_{SE}) and voltage reference dependent offset voltages (included in V_{SI}). The groups were formed so that commonly known quantities could be used to form the various parameters required for this error analysis. Another reason to group these quantities, is that variations within a group would produce similar effects on the conversion process. For the two conversion methods considered, the worst case error varies with the applied signal. This initially suggests the case where a subtraction occurs in every stage, causing more error sources to contribute to the overall error. The above subtraction procedure should result when the input is set to the highest quantization level so that all bits become one.

After the initial delay, the processed input arrives at the output of the last full stage which is referred to as V_{EXP}. This voltage can be represented by

$$V_{EXP} = V'_{IN}K_S{}^n - \lambda K_R V_{SI}[K_S{}^n + K_S{}^{n-1}2^{-s} + \cdots$$

$$+ K_S 2^{-s(n-1)}] - \lambda V_{SE}[K_S{}^n + K_S{}^{n-1} + \cdots + K_S] \qquad (2.1)$$

for the series-flash converter if V_{IN} is at the highest quantization level. Arithmetic manipulation of (2.1) results in

$$V_{EXP} = V'_{IN}K_S{}^n - \lambda V_{SI}K_R \frac{K_S{}^n - 2^{(r-N)}}{1-(K_S 2^s)^{-1}} - \lambda V_{SE}\frac{K_S{}^n - 1}{1-K_S{}^{-1}} \qquad (2.2)$$

It is assumed in (2.1) and (2.2) that $K_S \neq 1$, $n \geq 1$ where $n = (N-r)/s$, and

$$V'_{IN} = V_{REF}(1-2^{-N-1}), \qquad V_{SI} = V_{REF}(1-2^{-s}) + I_E.$$

Then (2.2) gives the worst value of V_{EXP} subject to the conditions shown. The extra non-ideal component V_{SE} is a consequence of stage offsets, charge injection and their correction voltages. In comparing (2.2) to the ideal value of V_{EXP}:

$$V_{EXPI} = V_{REF}(2^{-N+r} - 2^{-N-1}) \tag{2.3}$$

an error term δ may be evaluated. With this equation V_{EXP} can be broken into its ideal and error portions.

$$V_{EXP} = V_{REF}(2^{-N+r} - 2^{-N-1} \pm \delta) \tag{2.4}$$

Reworking (2.4) using (2.3) and (2.2) the normalized error term δ can be evaluated.

$$\delta = \left| (1-2^{-N-1})K_S{}^n - V_{SI}/V_{REF}\lambda K_R \frac{K_S{}^n - 2^{(r-N)}}{1-(K_S 2^s)^{-1}} - V_{SE}/V_{REF}\lambda \frac{K_S{}^n - 1}{1-K_S{}^{-1}} + 2^{-N-1} - 2^{-N+r} \right| \tag{2.5}$$

Similar manipulations for the algorithmic converter produce:

$$V_{EXP} = V'_{IN}(2^s K_S)^n - \lambda(K_R V_{SI} + V_{SE})[(2^s K_S)^n + (2^s K_S)^{n-1} + \cdots + 2^s K_S] \tag{2.6}$$

and

$$V_{EXPI} = V_{REF}(1-2^{-r-1}) \tag{2.7}$$

such that $n \geq 1$, $V'_{IN} = V_{REF}(1-2^{-N-1})$, and

$$V_{SI} = V_{REF}(1-2^{-s}) + I_E$$

This results in

$$\delta = \left|(1-2^{-N-1})(2^{s}K_{S})^{n}-\lambda\frac{(K_{R}V_{SI}+V_{SE})[(2^{s}K_{S})^{n}-1]}{V_{REF}(1-(2^{s}K_{S})^{-1})}+2^{-r-1}-1\right| \text{ such that } K_{S}2^{s}\neq 1 \tag{2.8}$$

for the algorithmic converter with the highest quantization level applied to its input.

With the normalized error δ, expressions (2.5) and (2.8), one can see how the various internal errors contribute to its value. If the stage gain errors (K_S) tend to reduce the input, and the other errors tend to reduce the subtracted signal at each stage a partial cancellation of these errors occurs. That is, a lower than normal input and subtrahend occurs at each stage. Therefore, the difference signal resulting is more accurate than it would be if one of the net errors had an opposite sign. To prevent this cancellation (worst case analysis) the subtrahend can be made zero by applying the lowest quantization level. Therefore, all bits should be zero. When the lowest quantization level is applied to the serial-flash converter,

$$V_{EXP}= V_{REF}2^{-N-1}K_{S}{}^{n}-V_{SEZ}\lambda\frac{K_{S}{}^{n}-1}{1-K_{S}{}^{-1}} \tag{2.9}$$

and

$$V_{EXPI}= V_{REF}2^{-N-1} \tag{2.10}$$

such that $K_S \neq 1$, $n \geq 1$, $V'_{IN} = V_{REF}2^{-N-1}$. Then for the series-flash converter,

$$\delta = \left| 2^{-N-1}K_S^{\,n} - V_{SEZ}/V_{REF}\lambda\frac{K_S^{\,n}-1}{1-K_S^{\,-1}} - 2^{-N-1} \right| \qquad (2.11)$$

Similarly, for the algorithmic converter

$$V_{EXP} = V_{REF}2^{-N-1}(2^sK_S)^n - \lambda V_{SEZ}\frac{(2^sK_S)^n-1}{1-(2^sK_S)^{-1}} \qquad (2.12)$$

$$V_{EXPI} = V_{REF}2^{-r-1} \qquad (2.13)$$

and

$$\delta = \left| 2^{-N-1}(2^sK_S)^n - \lambda V_{SEZ}/V_{REF}\frac{(2^sK_S)^n-1}{1-(2^sK_S)^{-1}} - 2^{-r-1} \right| \qquad (2.14)$$

Here $V_{SEZ} = V_{SE} - V_D < V_{SE}$, when no subtraction is performed.

2.3 COMPARATOR ERROR ANALYSIS

In the preceding discussion it was assumed that the internal series-flash A/D converter's comparator accuracy resulted in valid digital outputs. For this analysis the stage's components excluding the comparators are assumed ideal.

To meet the ±1/2 LSB linearity error criterion required of most converters, the first stage's comparators must have less than 1/2 LSB absolute error. Furthermore, if the comparators were now made ideal, a maximum offset voltage (due to error sources) equivalent to just less than 1/2 LSB could be tolerated, and still result in the specified error limit. Therefore, the next stage would see this offset voltage amplified $2^{s(1-a)}$ times, but still provide the correct conversion if its comparators were ideal. Again the offset error is interchangeable with the maximum comparator error tolerance, since only voltage differences are of importance.

By the above reasoning, an expression for the comparator tolerance requirement at any stage i is

$$V_{NI} = |2^{s(1-a)(i-1)-N-1}| \qquad (2.15)$$

This expression is normalized with respect to V_{REF}. If (2.15) is evaluated for the partial stage's comparators ($i = n+1$) the following results

$$V_{NP} = |2^{s(1-a)n-N-1}| \qquad (2.16)$$

When the converter's parameters are known, a normalized error value V_{CN} is easily obtained for the worst case comparison made within the partial stage's internal A/D converter's block. The value V_{CN} is considered a normalized sum of the comparator's and voltage reference's offset voltages. After a stage type has been decided on, with known parameters V_{CN}, V_{NP} and the maximum δ, a check may be made to see if the precision requirement in bits can be met.

When dealing with either of the fixed inputs the whole converter operates as a linear device. This implies that the superposition principle may be applied [HAYT,1978]. If

$$V_{NP}(1-2\epsilon)+V_{CN}+\delta<V_{NP} \quad (2.17)$$

such that $0\leq\epsilon\leq1/2$

is satisfied, the chosen wordlength is possible. This equation produces a valid result when the worst case δ is used, which is ordinarily not the case. It should be stressed that all full stages must produce S bits and all stages must have the same error tolerances. Expression (2.17) also insures that the maximum conversion error is less than ±(1/2+ϵ) LSB (again, only if the worst case δ is used).

2.4 SIMULATED STAGE ANALYSIS

The worst case δ is not at a fixed point for all stage parameter sets or wordlengths. Therefore, it is not possible to determine the maximum N unless additional steps are taken. To overcome this difficulty, a computer program was formed to simulate the errors considered in the above analysis. With this program and a parameter set, conversion can be simulated for all quantization levels and some intermediate values (depending on the accuracy desired) to yield the worst case conversion.

This process proceeds as follows: given a parameter set and a value of *s*, an input range is digitized ($n \geq 1$), if the maximum conversion error permitted has not been reached N is increased; if the maximum error has been exceeded use the previous value of N. To speed up this procedure the maximum value of N, resulting from the δ calculations, can be used to furnish the initial iteration point. Current work suggests that the δ method alone provides answers equal to or in excess (approximately less than 3 bits) of the desired maximum quantization error. That is, by calculating δ and then increasing N and/or *s* until the maximum permissible error is exceeded, a value of N from this iteration could be used as a starting point for the ADC simulation which requires more processing time.

The programs developed were initially written in BASIC but were rewritten in C language, because of the language's transportability and flexible structures. Several of the programs are included in appendix one. They include: a comparator analysis simulator; a ADC converter simulator; and a maximum wordlength determining ADC simulator. Both algorithmic and serial-flash converter architectures can be simulated in the last two programs. Only the algorithmic architecture is considered for the comparator simulation because this results in the only information that is not well documented, if at all, in literature.

In the first simulation, the program prompts for the required data. It then responds with the maximum permissible comparator offset for each stage used in the analog to digital conversion. The simulation assumes ideal devices are being used. To determine the maximum permissible comparator offset voltage all the discernible quantization levels are generated and an ideal converter simulation is then used to digitize the inputs. Throughout the simulation the minimum difference between all the comparators' reference voltages and the comparison voltage (the input voltage or partially processed input) for all the stages are recorded. After all the voltages have been simulated the minimum voltage differences are printed out. These values indicate the maximum permissible comparator offset voltages, therefore verifying the equation for the maximum comparator offset voltage tolerance (2.15).

The second simulation allows the user to simulate all the possible conversions for a given set of parameters, and the selected ADC's architecture. This simulation will printout the following every k^{th} point.

1. the k^{th} input voltage
2. the resulting conversion error in LSBs

The last result printed out is for the first occurrence of the worst case value of the above indicated printout. Facilities to simulate input values in between quantization voltages are also provided.

Using the stage simulator, the third program was constructed. It operates as was previously outlined. The included program does not incorporate the δ calculations to determine the starting point of the converter's maximum wordlength simulation. A wordlength larger than is possible for the set maximum permissible conversion error can be used in order to facilitate the future use of an initial N starting point provided by the δ calculations. The user may then locate the most likely region for the worst case δ of their architecture and parameter set using the maximum wordlength or stage simulator, and then use the N from their δ calculations for the starting value. This should speed up the simulation considerably because for each bit in the wordlength some 2^N*INC conversion simulations must be performed. Here INC is the number of divisions taken between adjacent quantization levels.

2.5 ERROR ANALYSIS CONCLUSION

It has been shown that the normalized error V_{NI} can be tolerated at any stage i (with ideal comparators). Furthermore the normalized error δ has been calculated, which is due to stage inaccuracies. The δ formulae give an indication of how various error sources cancel with different parameter sets and word lengths. An error analysis technique is demonstrated that provides a rough estimate to the maximum N available. A software simulation of the converters is required for more precisely determined maximum wordlengths.

With respect to the proposed pipelined algorithmic structure, offset errors are predominantly due to internal offset voltages. While gain errors are due to interstage gains and reference voltage errors. Linearity errors are usually due to the combination of internal gain, offset voltage and reference voltage errors. The differential nonlinearity errors are due to different polarity and accumulations of the linearity error sources in adjacent stages.

3. HIGH SLEW RATE/LOW POWER BUFFER AMPLIFIER DESIGN

The constraints placed on the ADC design set out in the introduction included:

1. rapid conversion $f_s > 100$ KHz
2. low power consumption

These specifications require carefully designed operational amplifiers, as they are the largest power consumers in the analog to digital conversion process. The conversion rate is also very dependent on the op-amps used, because they are connected one after the other within a full stage. Therefore, decreasing the time the op-amps have to slew will speed up the overall conversion process.

Most of the op-amps used in the proposed ADC are configured as buffer amplifiers (gain of 1). These buffer amplifiers are used in the S&H and subtractor circuits where the loads are capacitive. Therefore, the approach taken in solving the above problem was to implement a dedicated buffer circuit rather than a general purpose op-amp configured as a buffer. This resulted in a CMOS design with similarities to a bipolar and JFET voltage follower reported by George Erdi [ERDI,1979].

3.1 FUNCTIONAL DESCRIPTION

The simplified circuit given in figure 3.1 is used to describe the buffer circuit's operation and characteristics. The input stage of the buffer consists of a source follower (M_1) in one branch and two diode connected MOSFETs (M_2,M_3)

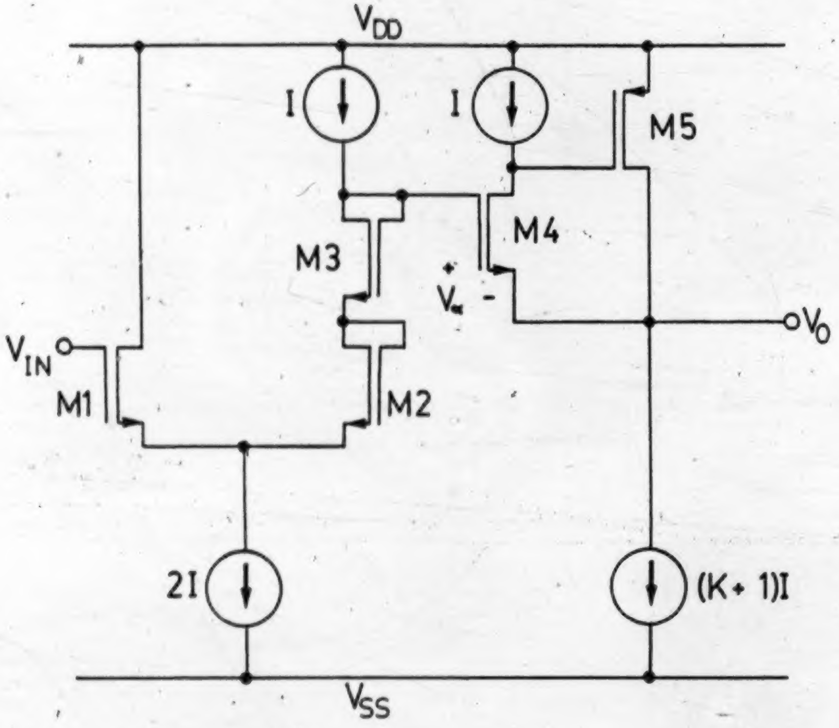

V_DD
I
I
M5
M4
M3
+
V_a
-
V_IN
M1
M2
V_O
2I
(K+ 1)I
V_SS

Figure 3.1 Simplified buffer circuit

in the other. Current is kept constant in the branches via the tail and branch current sources. All the N-channel transistors shown in the figure have the same geometry. They produce the same gate to source voltage drop, because all conduct the same current level. This voltage drop will be referred to as V_a on these and any other identically matched MOSFETs conducting current *I*. The input stage level shifts the input voltage up by V_a.

In the second stage another source follower (M_4) is employed. This stage drops the previously up-shifted input voltage by V_a. Therefore, this stage's output returns to the same value that V_{IN} is at.

To explain how the output stage boosts the current, a change in this stage's input voltage will be followed to the output. Assume the voltage level has just changed on the gate of M_4. This produces a change in V_{GS4} because the output voltage cannot change instantaneously due to the load capacitance. Therefore, the modification of M_4's V_a results in a change of the current flowing through M_4. The change in I_{s4} attempts to alter the current from the high output impedance current source connected to M_4's drain. This produces a voltage change at the gate of M_5. Transistor M_5 will then produce the current necessary to move the buffer's output voltage so that V_{GS4} returns to its nominal value of V_a. Steady state operation is always achieved when M_5's gate has been adjusted so that current *I* produced by the current source driving M_4 is able to flow through M_4's drain.

This buffer is designed to provide a voltage output using current sources as drivers and current feedback for regulation of the output's voltage. The current sources are used as the output drivers so that capacitive loads can be driven directly from a current source rather than a voltage source which reverts to a current source. Present designs sometimes do use this approach, but the output's voltage level control is achieved by providing overall voltage feedback to the input of the op-amp. This leads to larger phase delays and slower transient responses than the feedback within the stage approach taken for this buffer amplifier.

The buffer amp's slew rate with no load is determined by the ability of the internal current sources to supply charge to the gates of transistors M_2, M_3, M_4 and M_5. If the general purpose op-amp approach was taken the internal current sources would have to supply charge to the transistor gates and a compensation capacitor. Because no feedback is employed across the entire amplifier, no compensation capacitor is required to insure the buffer amplifiers stability. The predominant factor in determining the buffer's slew rate is the load's capacitance and the current producing capabilities of M_5.

3.2 BUFFER OPERATION IN DETAIL

The source follower is used in two key sections of the buffer amplifier design. It can take on one of the configurations shown in figure 3.2. Each is driven with a voltage source with an output resistance of r_s. For analog designers a common connection between the source and substrate is usually preferred, because this leads to a lower effective V_t and a more precise gain [GRAY,1984;GREBENE,1984]. Undesirable side effects result when using this configuration to drive capacitive loads at high frequencies, a fact not well detailed in literature. When the common source and substrate connection source follower drives a capacitive load, a resonant peak in the transfer characteristic may form. This resonant peak increases the settling time for output transitions.

Analysis of the output impedance using the models of the source followers also indicated in figure 3.2 gives:

$$Z_o = \frac{1+C_{gs}r_s s}{C_{gs}(r_s/r_{ds}+1)s+g_m+1/r_{ds}} \tag{3.1}$$

for the common source and bulk configuration and,

$$Z_o = \frac{1+C_{gs}r_s s}{C_{gs}(r_s/r_{ds}+g_{mb}r_s+1)s+g_m+1/r_{ds}+g_{mb}} \tag{3.2}$$

for the separate source and bulk connections. In either case the output impedance has the same inductive component associated with it.

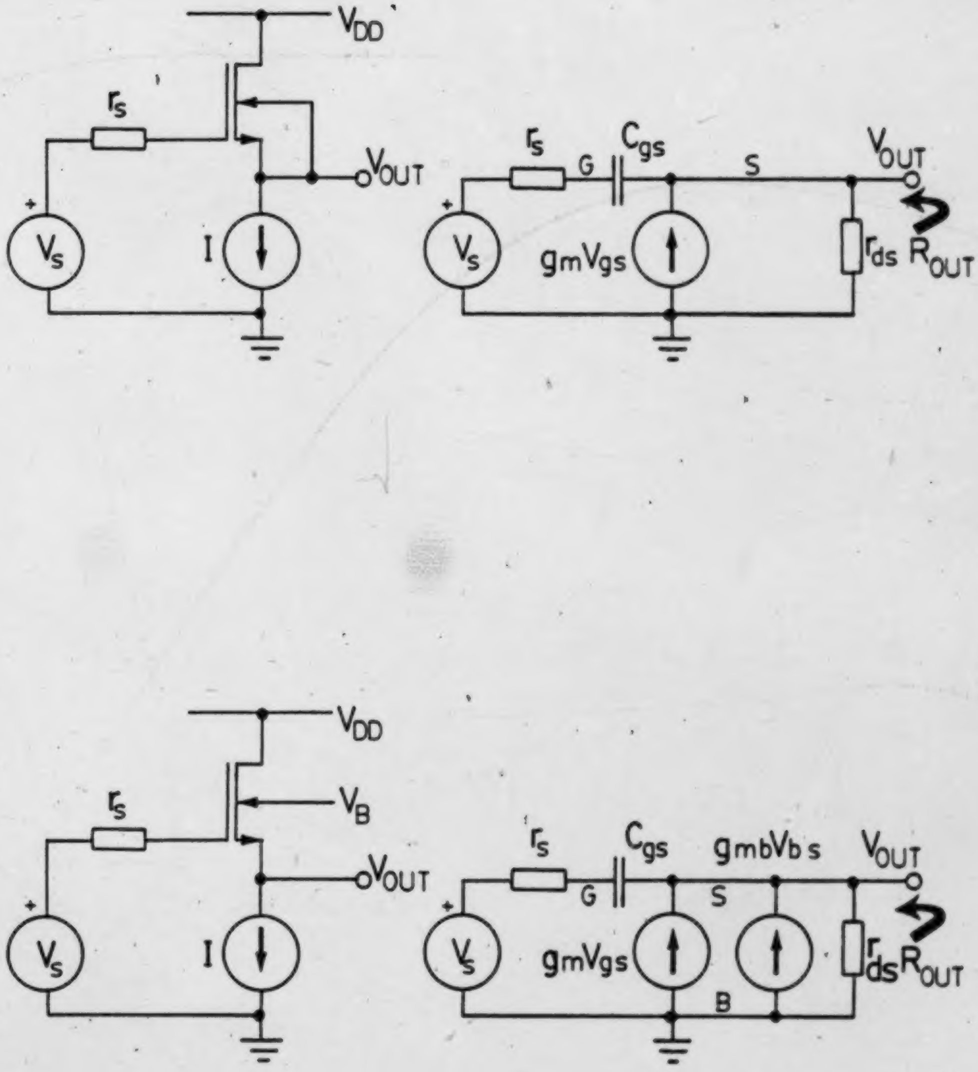

V_{DD}
r_s
V_{OUT}
+
V_s
I
r_s
G
C_{gs}
S
V_{OUT}
+
V_s
g_mV_{gs}
r_{ds}
R_{OUT}
V_{DD}
r_s
V_B
V_{OUT}
+
V_s
I
r_s
C_{gs}
$g_{mb}V_{bs}$
V_{OUT}
G
S
+
V_s
g_mV_{gs}
r_{ds}
R_{OUT}
B

Figure 3.2 Source follower configurations:(a) with common source and substrate connection;(b) with separate source and substrate connections.

When the source and substrate are separated an additional parallel resistance component, due to the bulk transconductance g_{mb}, reduces both the output impedance and the pole frequency of the output resistance function. This result eliminates the peak in the gain versus frequency characteristic when the source follower is used to drive capacitive loads. That is, a gain above 0 dB does not occur for this configuration as it does when there is a common source and substrate connection for load capacitances of 1pF or less.

3.2.1 OFFSET VOLTAGE REDUCTION

To reduce the voltage offset that occurs when using this buffer amplifier, V_a must be maintained throughout the entire input range. The value may vary but a loop analysis from the input to the output of the circuit should result in no voltage difference. As a result of providing a separate substrate bias for the signal path transistors, V_a is not identical for M_1, M_2, M_3 and M_4. Instead V_{GS} is matched for MOSFET pairs. That is, transistor pairs M_1, M_2 and M_3, M_4 should have identical V_{GS} voltage values.

The complete schematic to this point is given in figure 3.3. In order to insure matched device pairs, the pairs must be geometrically and electrically identical so that the same voltages occur on their electrodes. If V_{DS} is kept identical for the matched pairs the current component due to their finite output impedance will be the same. Two transistors,

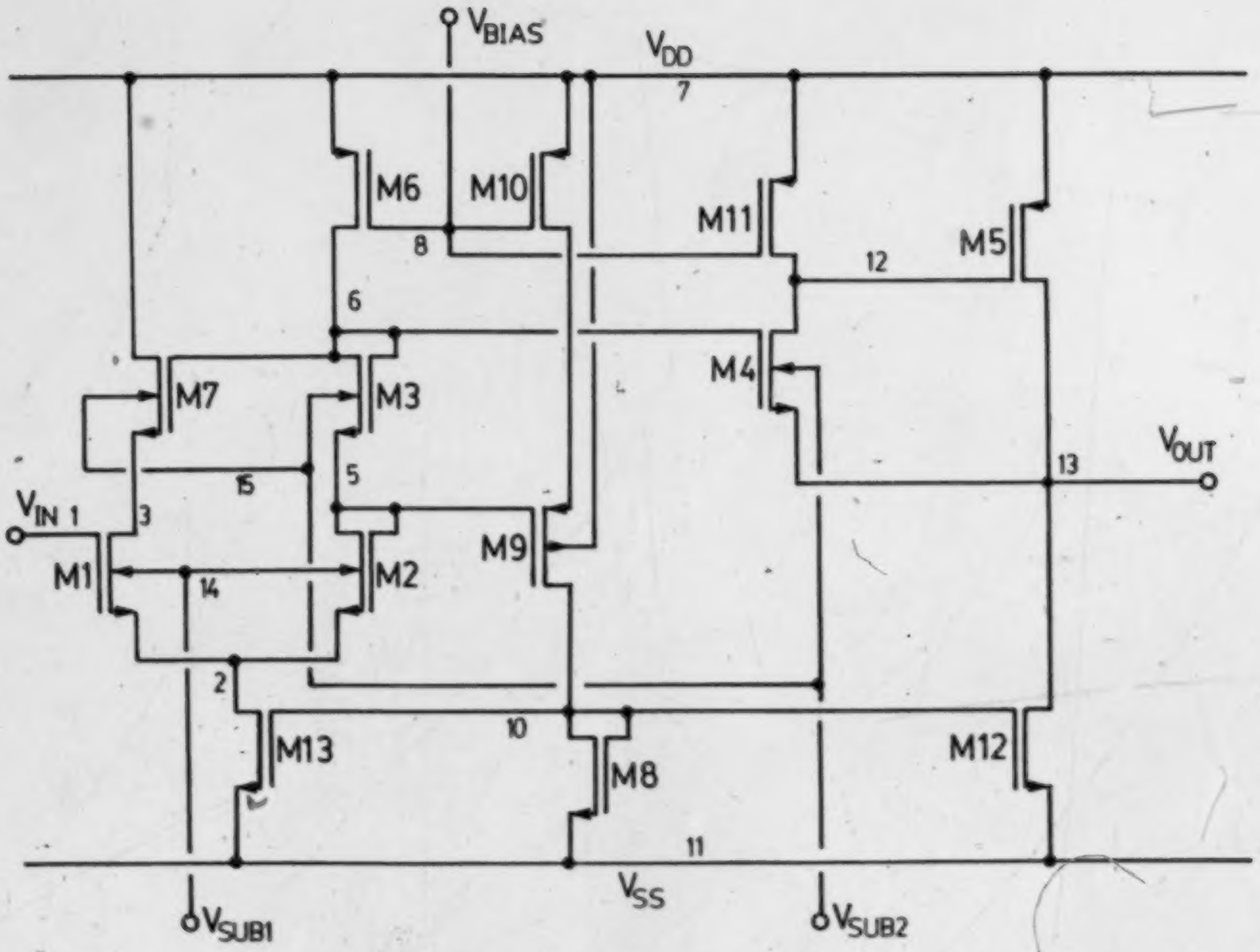

V_{BIAS}
V_{DD}
7
M6
M10
M11
M5
8
12
6
M7
M3
M4
15
5
V_{OUT}
13
$V_{IN\ 1}$
3
M1
14
M2
M9
2
M13
10
M8
M12
11
V_{SS}
V_{SUB1}
V_{SUB2}

Figure 3.3 Phase two buffer amplifier configuration

M_7 and M_9, are added for this reason. The drain to source voltage of M_2 is replicated across its pair M_1 by the source follower M_7. Similarly, the drain to source voltage of the branch current source transistor M_6 is replicated across M_{10} by M_9. Transistor M_{10} is used to mirror the input stage's right branch current in order to form a tail current of twice its value.

The voltage variation at node 12 encompasses a large range because M_5's gate can be set so that transistor M_5 is either fully on or cut off. For this reason, transistors M_{11} and M_4 have their length increased. Accordingly, voltage variations across their drain to source connections have less of an effect on their drain currents. Therefore, M_{11} will have a larger gate length than M_6, as will M_4 compared to transistors M_3 and M_7. It may be advisable to keep M_3 and M_4 identical for better matching though. Source follower M_9 does not replicate V_{DS6} across M_{10} very accurately because M_9's threshold voltage varies due to the body effect as its source potential changes. For this reason M_{10} also has a larger gate length in comparison to M_6.

3.2.2 PRELIMINARY CONCLUSIONS

Using the 'SPICE' circuit simulation package, the circuit configuration previously given in figure 3.3, was simulated [VLADIMIRESCU,1981]. Some of the data obtained is included in appendix two. The DC analysis shows how the buffer responds to a varying input voltage. This circuit is designed to work for an input range extending from 0 to 2 volts. Therefore, values that go beyond this range are included only to indicate possible trouble spots if this design is modified to extend its input range. The DC analysis also reveals a problem with this circuit's configuration. That is, as the input voltage varies so does the amount of voltage offset. Therefore, a voltage offset reduction method would only be partially successful because the correction voltage is uniquely correct for a particular input value. This will reduce the maximum number of bits obtainable when the buffer is employed in the proposed ADC.

The next analysis performed, AC analysis, is used to determine the amplifier's gain versus frequency response. One graph of the frequency response for the buffer using the source follower with a common substrate and source connection is also included so that the peaking due to the excessive output inductance can be observed. A satisfactory gain bandwidth product is obtained with the separate substrate and source connection. The value of the gain approximately corresponds to a general purpose amplifier with a gain of 57 and a BW of 110 KHz configured as a unity gain amplifier. Although a higher precision unity gain is desirable, the gain error can be partially compensated for by the precision gain amplifier that provides the stage's gain.

In the final simulation a transient analysis is performed. From this data it is clear that the buffer's slew rate is higher than is usually possible for a general purpose amplifier configurated as a unity gain amplifier operating at the same current level [GRAY,1984]. The settling time and the overshoot is longer and larger, respectively, than is expected from looking at the AC analysis characteristic.

3.3 OFFSET VOLTAGE REDUCTION AND GAIN ENHANCEMENT

Both the varying offset voltage and low gain accuracy problems are reduced by implementing the same subcircuit which consists of an over-compensated transconductance amplifier. This subcircuit is included with the previously used simplified buffer circuit in figure 3.4 to provide a more readily understood explanation of the entire circuit's operation. The transconductance amplifier's output is connected to the drain of M_3 so that the right hand branch current can be modified by the subcircuit. By changing the right hand branch current, the left hand branch current is also changed such that the sum of the branch currents equals the current requirement of the tail current source, which is fixed. When the branch currents are varied, V_{GS} of M_1, M_2 and M_3 also vary. This in turn alters the buffer's output voltage.

To reduce the variation in the present buffer's offset voltage, the added subcircuit is configured as a negative feedback amplifier. The subcircuit adjusts the branch current so that there is no voltage difference between its

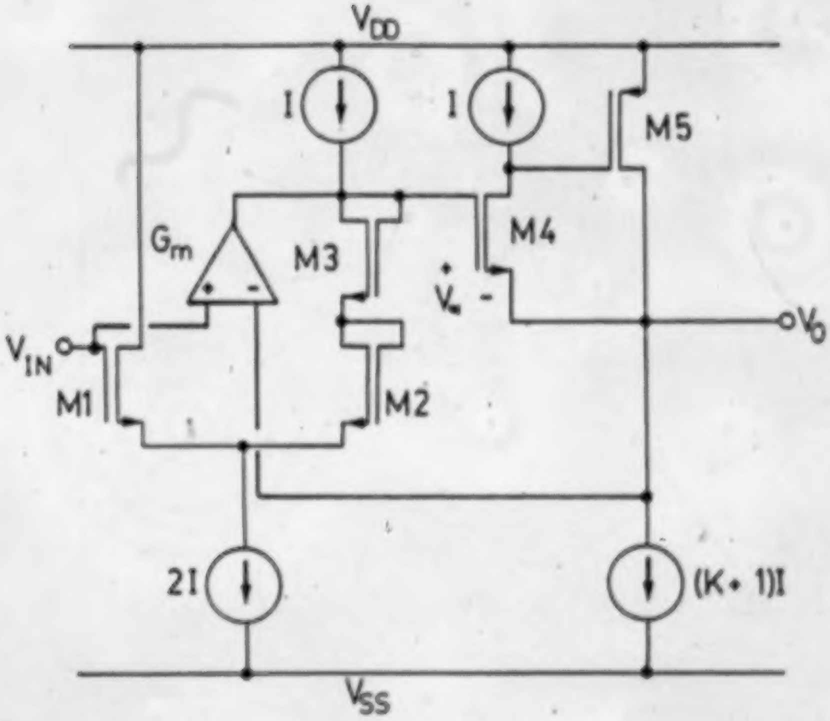

V_DD
I
I
M5
G_m
M3
M4
+
V_a
-
V_IN
M1
M2
V_o
2I
(K+1)I
V_SS

Figure 3.4 Simplified diagram of the buffer amplifier and its subcircuit

inputs. Therefore, since its inputs are connected to the buffer amplifier's input and output, there should be no voltage difference between these points for the ideal case. This method can then reduce the gain and offset voltage errors as is required.

The transconductance amplifier is over-compensated to insure that its contribution to the buffer amplifier's output does not influence the buffer's overall stability. This technique allows the faster original portion of the buffer to slew rapidly to its steady state value which is in error because of the voltage offset and the imprecise gain. The slower subcircuit then responds to the error present and adjusts the output to a more precise value. The small voltage error present after the original buffer amplifier has slewed is reduced in a short time even with the slower subcircuit's slew rate, because it does not have far to go.

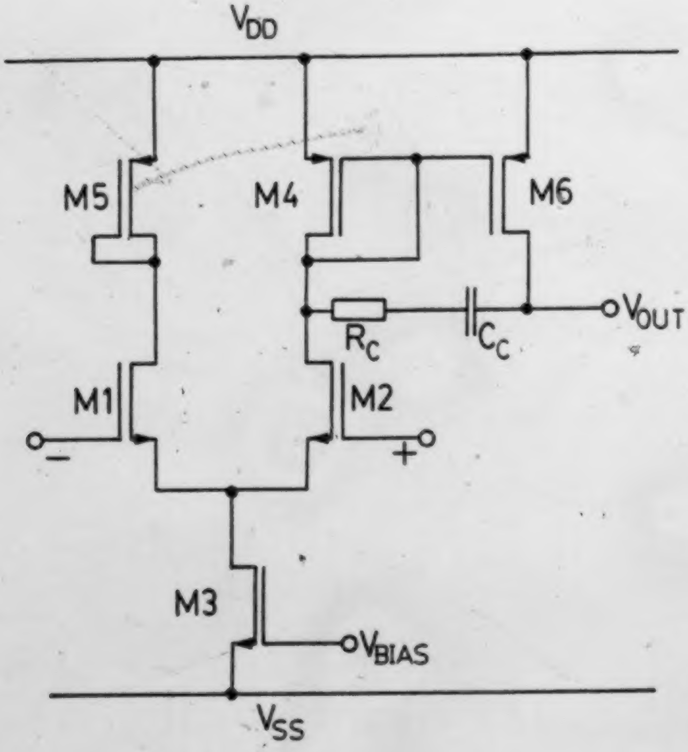
When implemented the transconductance amplifier can take on two distinct forms. It may provide a current output of both polarities or just of one. If the single polarity output transconductance amplifier is chosen then the die area required for its construction is reduced. There is a savings of approximately three transistors when going from a dual polarity (nine transistors) to a single polarity (six transistors) output. To do this, a nonsymmetric buffer input is required. That is, different values of bias current will flow through the buffer's input branches until the subcircuit compensates for the difference. The branch current that the transconductance amplifier directly modifies must be at a value which can be varied in only a single direction by the subcircuit.

3.4 BUFFER SUBCIRCUIT DESIGN

A unipolar output transconductance amplifier was used to verify the above claims of improved performance. Figure 3.5 illustrates the transconductance amplifier chosen to obtain the simulated data. The device can only source current, and it also provides a constant current with its inputs at the same voltage level. Therefore, the current source supplying the current to the right hand branch of the buffer would have to be reduced by the amount added by the subcircuit. In fact, the right hand branch current source may be removed if the subcircuit is biased at the appropriate level.

The transconductance amplifier is kept as simple as possible so that the die area it takes up is low. Furthermore, no attempt was made to optimize either the subcircuit or the entire enhanced buffer. This step in the buffer's design would take place once the fabrication process parameters are known.

The subcircuit's input stage consists of a differential pair. Transistor M_4 mirrors the right hand branch current to the output transistor M_6. The left hand branch's diode connected transistor M_5 is used to reduce the voltage drop across M_1, and therefore the current error due to M_1's



V_{DD}
M5
M4
M6
R_C
C_C
V_{OUT}
M1
M2
−
+
M3
V_{BIAS}
V_{SS}

Figure 3.5 Unipolar transconductance amplifier

output resistance. Compensation of the subcircuit is realized by taking advantage of the Miller effect by connecting a capacitor and resistor in series between the circuit's output and M_4's drain.

3.5 THEORETICAL CALCULATIONS

Some theoretical calculations that will increase the understanding of the buffer amplifier are presented in this section (refer to figure 3.3). Before the subcircuit was in place the buffer's gain was determined by the input stage's source follower gain in series with the output stage's gain. The input and output stages' gains are given by

$$A_{INPUT} \simeq 1+g_{mb3}/g_{m3} \qquad A_{OUT} \simeq \frac{1}{1+g_{mb4}/g_{m4}} \qquad (3.3)$$

To arrive at these approximations it was assumed that $r_{ds6} >> 1/g_{m3}$ for the input stage, and that the output stage was not loaded. The equations do take the body effect into account. Therefore, the buffer's gain becomes

$$A_{OBUF} \simeq \frac{1+g_{mb3}/g_{m3}}{1+g_{mb4}/g_{m4}} \qquad (3.4)$$

When the subcircuit is connected, the buffer's gain accuracy is increased. The buffer's two stages and its subcircuit are shown in figure 3.6. With the subcircuit removed, the block diagram reverts to the original buffer's form. The buffer's first stage has a finite output resistance. This does not

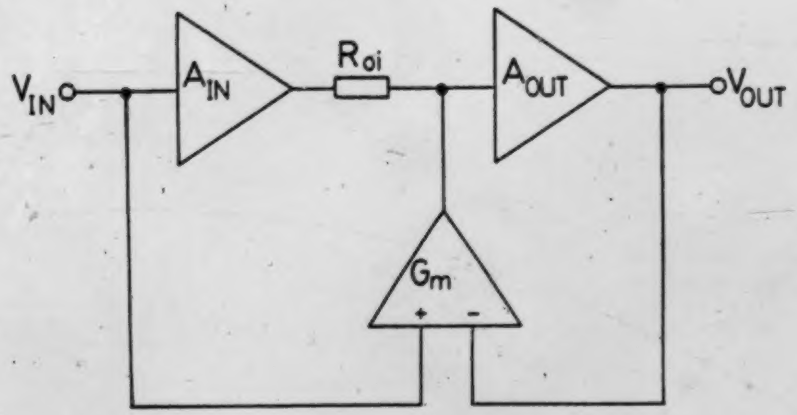

V_IN
A_IN
R_oi
A_OUT
V_OUT
G_m
+
-

Figure 3.6 Enhanced buffer amplifier block diagram

affect the gain of the original buffer because the input resistance of the output stage results in negligible loading. However the first stage's output resistance permits the subcircuit to modify the buffer's gain. Using the superposition theorem, the net effect of the subcircuit can be calculated. The buffer's gain becomes

$$A_{BUF} = A_{OBUF} \frac{1+G_m R_{oi} / A_{INPUT}}{1+G_m R_{oi} A_{OUT}} \tag{3.5}$$

where R_{oi} is the first stage's output resistance and G_m is the transconductance of the subcircuit. The output resistance is given by

$$R_{oi} = 1/g_{m3}(1+(g_{m3}+g_{mb3})2/g_{m1}) \tag{3.6}$$

The subcircuit's transconductance has a value of

$$G_m = \frac{g_{m1} g_{m6}}{2g_{m4}} \tag{3.7}$$

The subcircuit adds to the buffer's output a value that is proportional to the amount of error present at the buffer's output.

An important consideration in the design of an open loop buffer is its output resistance. If a large bandwidth is obtained the effective BW may be reduced by a high output resistance because of the time constant formed when driving a capacitive load. With the current feedback used in this buffer's output stage, its output resistance produces a negligible time constant. The output resistance of the buffer without the subcircuit is given by

$$R_o \simeq \frac{1 + r_{ds11}/r_{ds4}}{(g_{m4}+g_{mb4})(1+g_{m5}r_{ds11})} \qquad (3.8)$$

A second benefit produced by the subcircuit is a reduction in the already low output resistance. The output resistance becomes

$$R_o \simeq \frac{1+r_{ds11}/r_{ds4}}{(g_{m4}+g_{mb4})(1+g_{m5}r_{ds11})+G_m(1+r_{ds11}/r_{ds4})} \qquad (3.9)$$

3.6 ENHANCED BUFFER AMPLIFIER CONCLUSIONS

The additional simulated data included in appendix two was obtained by connecting the previously designed subcircuit, as described in the section on offset voltage reduction and gain enhancement. The same analysis is performed on the modified buffer as was done on the original.

The DC analysis produces data that indicates the subcircuit increases the offset voltage but it is now far less dependent on the buffer's input voltage. This result implies that the wordlength obtainable will be increased if offset correction procedures are also implemented.

Data produced by the AC analysis also indicates almost a one order of magnitude increase in the gain of a general purpose op-amp equivalent configured as a voltage follower.

The gain bandwidth product remains essentially the same. This new data indicates a general purpose amplifier with an open loop gain of 422 and roughly a 110 KHz bandwidth should produce a similar closed loop frequency response.

The following table is a compilation of data produced when the buffer was simulated. Because all the simulations required did not converge, for no apparent reason, some of the data include in the table is determined by observing the trends in simulations that did produce results.

3.7 SWITCHABLE OUTPUT BUFFER MODIFICATION

As an added benefit of driving the buffer's load with current sources, the output circuitry can be modified to permit the output to enter a high impedance state. That is, it will appear as if the buffer had a switch in series with its output. This technique is not used for the proposed ADC, because it would make the bias circuitry more complex. However, for some implementations this technique may prove useful and is therefore worth mentioning.

Using the following technique the component count and power consumption may be reduced. Furthermore, the settling time and charge injection of a S&H circuit employing the buffer may also be reduced. This modification can be made by inserting transistor M_{15} as a digital switch between nodes 7 and 8 of figure 3.3. This switch can then switch the buffer's entire operating current off, therefore cutting off the output stage's transistors. This assumes that the bias

Table 3.1 Buffer amplifier parameters

PARAMETER[†]	**UNMODIFIED BUFFER VALUE**	**MODIFIED BUFFER VALUE**	**UNIT**
V_{os}	19 to 28	26 to 24	mV
gain	-0.15106	-0.02061	dB
slew rate	-15,+16	-14,+22	V/µS
BW	6.3	6.0	MHz
power[*]	822	866	µW

[†] the input range is from 0 to 2 volts, with the current I approximately at 17µA and a load capacitance of 1pF.

[*] less repetitive circuitry

voltage source across nodes 7 and 8 can be shorted, or that the bias voltage source can be set to produce a zero voltage difference.

4. PRECISION GAIN AMPLIFIER DESIGN

An accurate value of the stage gain is required for serial ADCs, because gain errors increase the overall error exponentially. To provide a precise stage gain without using trimmed resistors, an electronically calibrated *precision gain amplifier* is proposed.

The schematic of the precision gain circuit is given in figure 4.1. Resistors R_A, R_B, and R_C are used to set the closed loop gain of OP_1. Transistor M_1 is operated in its triode region so that it behaves like a resistor. During the gain calibration procedure, V_{IN} is held at $V_{REF}/2^s$, where 2^s as before is the required stage gain. The switch is closed during a calibration procedure so that the gate of M_1 can be varied by the output of OP_2. As M_1's gate voltage is varied, its drain to source resistance also varies. This in turn changes V_O until ideally the difference between the differential inputs of OP_2 becomes zero. At this point the gain would be at the required value. When the switch is opened at the end of the calibration interval the voltage on M_1's gate is held by a capacitor. The precision gain amplifier may then be used in the analog to digital conversion process.

To determine the values of the components in this circuit, the stage's gain (equation 4.1) will be set at the required value of 2^s for two extreme cases in component tolerances. It is therefore assumed that tolerance values in between the extreme cases will also be compensated for. The

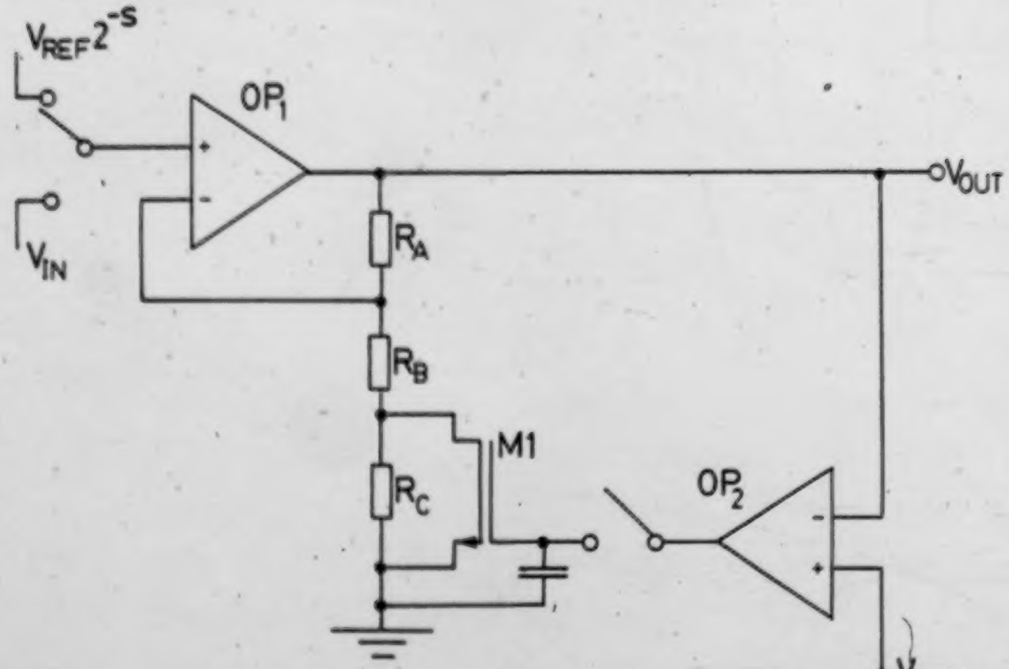

$V_{REF}2^{-s}$
OP_1
+
-
V_{IN}
V_{OUT}
R_A
R_B
R_C
M1
OP_2
-
+
V_{REF}

Figure 4.1 Precision gain amplifier

lowest gain occurs when the numerator of the gain expression is at its lowest and when the denominator is at its highest. If valid components are chosen, the effective resistance between the drain and source of the transistor, henceforth referred to as R_X, will be able to compensate for the other component errors. That is, the resistance of R_X in parallel with R_C should be able to reduce the denominator sufficiently to result in the required gain. This equivalent resistance is denoted as R_p. To arrive at the circuit's gain the following formula may be used:

$$\text{gain}=\frac{A_{OL}}{2^{s}+A_{OL}}\left(1+\frac{R_A}{R_B+R_p}\right) \tag{4.1}$$

It may then be set to produce the compensated minimum gain expression which is given by

$$A_{MIN}=\frac{A_{OL}}{2^{s}+A_{OL}}\left(1+\frac{R_A(1-p)}{R_B(1+p)+qR_C(1+p)}\right) \tag{4.2}$$

where p is the resistor tolerance, q is a factor which indicates how much the lowest available R_X in parallel with R_C reduces R_C's value, and A_{OL}, which is OP_1's open loop gain. The values of p and q may be calculated as follows:

$$p=\frac{\Delta R}{R} \tag{4.3}$$

and

$$q = \frac{1}{1+R_C/R_{XMIN}} \tag{4.4}$$

where R_{XMIN} is the lowest resistance R_X can be set at. This value is given by

$$R_{XMIN} = \frac{1}{C_{ox}\mu_n W/L(V_{DD}-V_t-V_{DS})} \tag{4.5}$$

At the other extreme a maximum compensated gain given by

$$A_{MAX} = \frac{A_{OL}}{2^s+A_{OL}}\left(1+\frac{R_A(1+p)}{R_B(1-p)+R_C(1-p)}\right) \tag{4.6}$$

occurs. In this expression, R_X has been set very much larger than R_C.

To provide compensation from A_{MIN} to A_{MAX}, both of the gains will be made equal to the required value. Arithmetic manipulation of this equality provides the following relationship,

$$R_B = \frac{R_C}{4p}[(1-q)(1+p^2)-2p(1+q)] \tag{4.7}$$

To form an equation that relates R_A to the above determined quantities the gain expression is used(4.1). The finite gain of OP_1 is taken into account, but the desired closed loop gain is set at 2^s instead of its nominally higher value. This leads to

$$R_A = [R_B+R_C(1+q)/2][2^s(2^s/A_{OL}+1)] \tag{4.8}$$

The average value of R_p was used for this calculation.

With the above formulae, a set of resistor values can be arrived at. An iterative process could be used to converge on a valid data set. The procedure could begin by choosing a value for the W/L ratio of the transistor and a value for R_C. With this data, both R_{XMIN} and q can be calculated. This then leads to the values of R_B and R_A. If an additional relation that relates R_C or R_{XMIN} to R_A is formed an iteration process can then begin.

4.1 SYSTEM STABILITY

At first glance the precision gain circuit appears to be unstable because the circuit seems to contain two op-amps in series during its calibration interval. After a closer inspection the circuit's stability can be shown. When the circuit is in its normal operation mode (used as a stage gain), the circuit's stability is insured if an over-compensated op-amp is used for OP_1. If a high stage gain is necessary, then a fully compensated OP_1 is not required, because the high gain requirement reduces the excess loop gain. A decrease in the excess loop gain will increase the precision gain circuit's stability [OGATA,1970]. Therefore, the compensation pole frequency can be increased as well as the system's frequency response by using an appropriately compensated op-amp [OGATA,1970].

It can be seen that for a properly set up system the open loop gain for the path that includes both the op-amps in series is given by,

$$A_{OL} = (A_{MAX} - A_{MIN}) \qquad (4.9)$$

The reason the gain is not higher, even though the full gain of OP_2 is included in the path is that the system is only designed to vary $1/\beta$ of OP_1, and hence its gain, between A_{MAX} and A_{MIN} with the required value being 2^s. The above expression may be rewritten as

$$A_{OL} \simeq 4\frac{\Delta R}{R}2^s \qquad (4.10)$$

This results in A_{OL} gains which are low, and usually well under 20 dB. The excess gain is easily reduced by the holding capacitor used and OP_2's output resistance, well before the system's phase margin causes concern.

The precision gain calibration takes advantage of OP_2's high open loop gain but insures system stability during the calibration interval by limiting the maximum change OP_2 can affect OP_1's $1/\beta$.

4.2 ERROR SOURCES

The main error sources during the precision gain calibration sequence are OP_1's and OP_2's offset voltages. The other less predominant error source is OP_2's finite open loop gain. These error sources result in the following overall gain accuracy if valid components were selected as detailed in a previously discussed section. That is, if the values used were derived using the formulae previously discussed, the following error expression is valid:

$$\text{error}= \left[1-\frac{A_{OL}(1+V_{os}/V_{REF})}{(1+A_{OL})(V_{SE}/V_{REF}2^{5}+1)}\right] \qquad (4.11)$$

where A_{OL} is OP_2's open loop-gain and V_{os} is its offset voltage. The term V_{SE} is an offset voltage error that is added to the required calibration voltage. To reduce these errors a special purpose op-amp has to be used. The device must reduce its error sources by an offset cancellation method and by designing it to have a high gain. Such an op-amp design has been reported by P.W. Li et al. [LI,1984]. The device has a gain larger than 92dB and can have its offset reduced by already known techniques [GREBENE,1984].

4.3 PRECISION GAIN CIRCUIT IMPLEMENTATION

It has been shown that the precision gain circuit can compensate for resistor tolerance errors. This circuit may also compensate for other circuit gain errors if this circuit's compensation range can be extended. That is, if a resistor tolerance error p can be chosen that is larger than the required value, the precision gain circuit's calibration range will be extended. Therefore, if the calibration voltage is first passed through other gain stages before it is connected to the precision gain circuits input, the circuit may be able to compensate for the previous gain errors. The resulting gain error of the entire network is given by (4.11) as well, if the same conditions are met.

5. PRACTICAL REALIZATION OF THE ADC

This chapter will bring together previously discussed circuits and information obtained, with additional circuits detailed here to illustrate the practical realization of the proposed ADC. To this point, an error analysis has been developed which indicated some specialized circuitry had to be designed, and on chip error correction had to be performed. Offset voltage errors will be dealt with in this chapter as will the subtractor and the S&H circuits. The analog delay's design will also be covered here.

5.1 THE SUBTRACTOR CIRCUIT

With the circuitry given in figure 5.1, a full stage, shown for $s=2$, can be realized. The design goals set out in this chapter's introduction can all be performed by a single circuit. The circuit will be referred to as the *subtractor*. This circuit consists of a buffer amplifier that charges a holding capacitor that can have its bottom plate switched between one of two potentials. Two of these circuits are in series, the first performs the subtraction operation while the second which also performs a subtraction reduces the stage's offset voltage errors. The two subtractor circuits together provide the analog delay function. This subtraction method appears to be the fastest and the least device dependent way to implement the desired functions.

At the beginning of a subtraction procedure a buffer amplifier's output is connected to the top plate of the

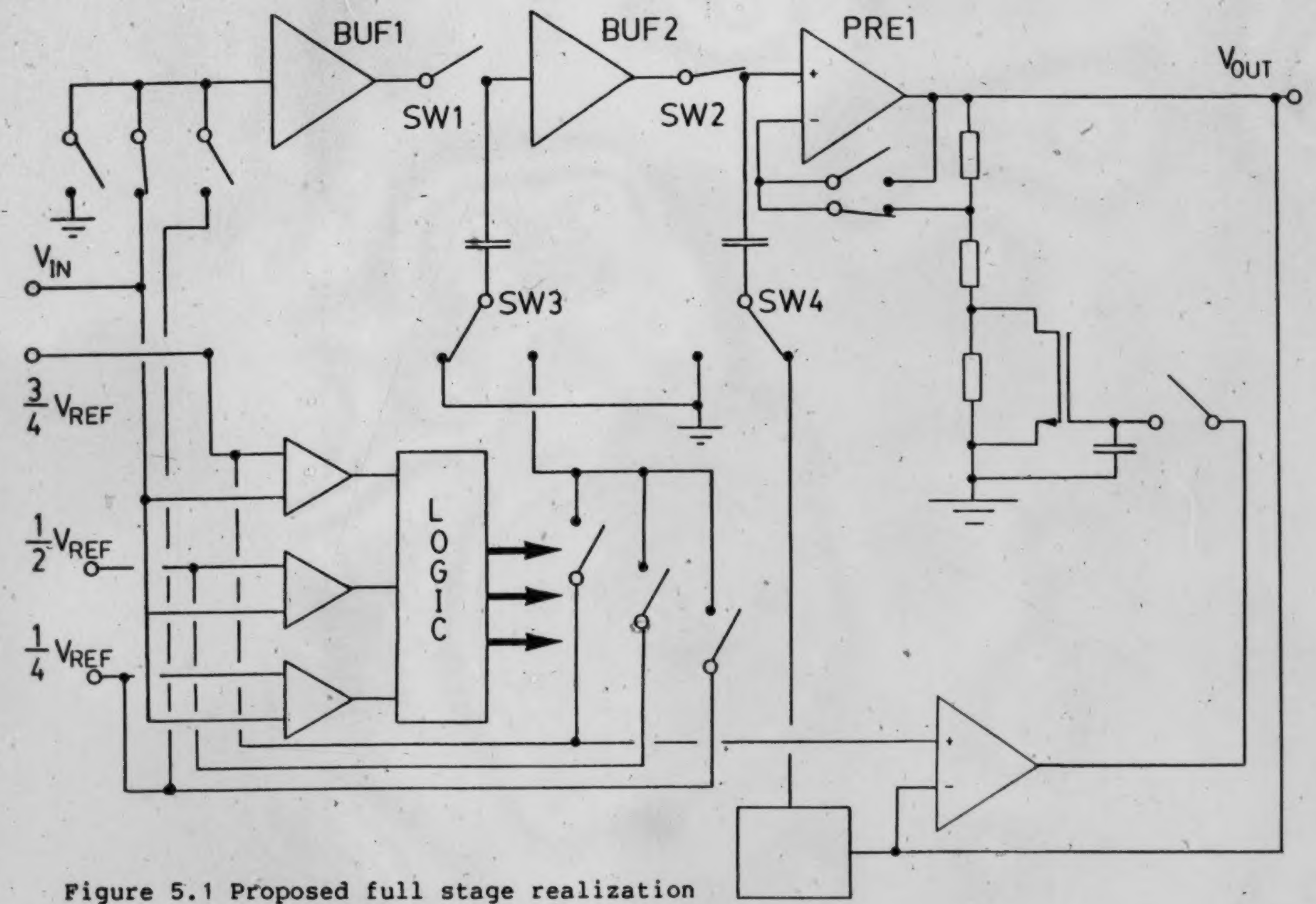

BUF1
BUF2
PRE1
SW1
SW2
SW3
SW4
V_{OUT}
V_{IN}
$\frac{3}{4}V_{REF}$
$\frac{1}{2}V_{REF}$
$\frac{1}{4}V_{REF}$
LOGIC
+
-

Figure 5.1 Proposed full stage realization

capacitor while the capacitor's bottom plate is held at the potential that is to be subtracted from the buffer's input. This first step produces the desired voltage difference across the holding capacitor. Once the difference voltage has stabilized, the buffer's output can be disconnected by opening the in series switch. Then the bottom plate of the capacitor is connected to the ground potential. Therefore, the desired difference signal will be present on the capacitor's top plate.

5.1.1 SUBTRACTOR ERROR SOURCES

Only one major error source exists for this subtractor. Any parasitic capacitance on the top plate reduces the amount subtracted from the input. The parasitic removes a charge proportional to the parasitic's size and the change in the sample capacitor's top plate voltage. This results in the following difference voltage during a subtraction procedure

$$V_{sub} = V_{IN} - V_d \frac{1}{1+C_p/C} \tag{5.1}$$

where V_d is the voltage to be subtracted and C_p and C are the parasitic and holding capacitor, respectively. The holding capacitor's bottom plate parasitic capacitance does not affect the difference voltage because the bottom plate is always set to a voltage potential.

The top plate's parasitic capacitance typically has a value of 0.1-1% of the actual capacitor value [GREBENE,1984]. This value may even be further reduced by careful layout and design techniques. If it can be arranged so that all full stage subtractors have the same sized parasitic capacitance the errors due to them may be reduced by increasing the value subtracted. Therefore, the subtrahend returns to its required value in the difference equation.

To a lesser degree switch charge injection also results in an error voltage. The error voltage resulting from charge injection may be reduced by using opposite polarity switching voltages of the same magnitude driving the CMOS switch. The switch must also have its transistor geometry set so that the charge contributed by the NMOS transistor is exactly cancelled by the contribution of the PMOS transistor. This is usually not done because the switch's resistance is not symmetric about an analog input range (about 0 volts). For this application the input's voltage symmetry is not important because only a single input polarity is being dealt with.

5.2 THE INTERNAL ADC AND DAC

In each full stage and the partial stage a flash converter will be used to produce the s and r bits, respectively. This conversion method was dealt with previously in the introductory chapter. As an added benefit resulting from the use of a flash converter, the full stage's DAC is easily constructed. The DAC can produce any of the possible output voltages by simply routing the appropriate fraction of V_{REF} used for the internal analog to digital conversion to the DAC's output using analog switches.

This digital to analog conversion method considerably reduces the amount of die area used compared to the alternative of arriving at the DAC's voltages independently. Another benefit of this technique is that the DAC produced voltages are always within the ADC's comparator's offset voltage of the digital value produced by the ADC. This should increase the number of bits possible compared to the other alternatives.

5.2.1 THE INTERNAL ADC'S COMPARATOR SELECTION

The ADC's comparator offset voltage may be reduced by using an error correction procedure. The best method appears to be one that is being used quite extensively in the construction of MOS converters already [DINGWALL,1979] [YEE,1978]. The references indicated do not use exactly the same method to realize a low offset voltage and high gain but they are quite similar.

To realize the comparator's high gain a noncompensated amplifier should be used. The simplest such amplifier is an inverter. Several inverters in series would increase the gain (see figure 5.2). To reduce the offset voltage a

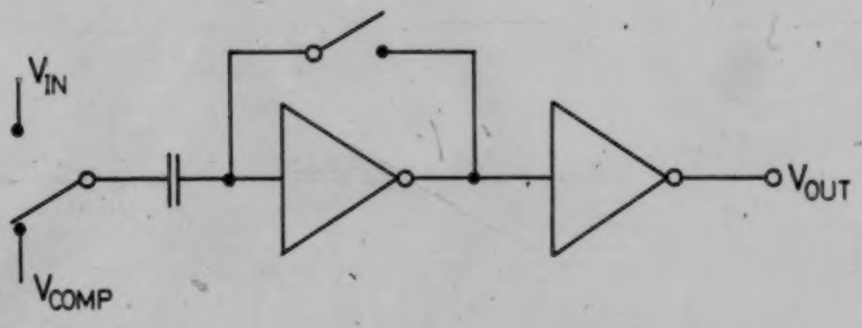

V_IN
V_COMP
V_OUT

Figure 5.2 Simple comparator with offset voltage reduction

capacitor would be connected between the input voltage and the first inverter. The first inverter would also have its output connected to its input. This procedure establishes the input voltage on one side of the capacitor and the first inverter's toggle voltage on the other. Then during the comparison procedure the connection between the first inverter's input and output is broken. Next the voltage that the input is to be compared to is connected to the side of the capacitor which was previously connected to the input. Therefore, the difference voltage less the first inverter's offset voltage is presented to the first inverter.

The overall offset voltage can be calculated by transferring the offset voltages of any additional inverters back through to the first. This would be done by dividing the additional stage offset voltages by the stage gains as they are passed back to the first inverter's input. For example if a two stage comparator is used and the second stage has an offset voltage of 40 mV, the effective offset voltage would only be 1 mV if the first stage had a gain of 40.

5.2.2 THE ADC'S REFERENCE VOLTAGES

The reference voltages required for the internal ADCs and DACs will probably not be included on chip. This will limit the number of bits the internal ADCs/DACs are capable of producing, because of the package's pin limitations. The internal data conversion circuits require 2^x-1 unique voltage reference fractions for an x bit word. This will probably limit the internal devices to a maximum wordlength of about 3 bits.

To generate the voltage reference fractions, a bipolar integrated chip would probably be used if two or more bits of internal data conversion were required. The separate chip would contain a stable reference voltage source driving a resistive divider which in turn fed some low voltage offset unity gain amplifiers. If only a single bit is internally determined an external potentiometer, discrete voltage reference and op-amp are required. An additional chip would require extra board space and a separate technology, but the main converter can still be made with the digital technology. There should still be a net savings, because the bipolar circuit is not extremely complicated and should have a high yield. Similarly the digital logic and ADC chip should have a high yield because of its on chip error correction. This contrasts with the other option which would have all the circuits on a single chip. The higher tolerances of the reference portion of the chip would both increase the cost of the process and decrease the yield.

5.3 FULL STAGE ERROR CORRECTION PROCEDURES

To produce a reasonable number of bits the proposed ADC has to reduce its internal errors by using an automatic error correction procedure. The various error corrections are performed alternately between valid samples and/or when the device being calibrated is not being used.

The first error correction procedure reduces the full stage's offset voltage. This procedure begins by setting BUF_1's input to the ground potential. The potential is then passed through BUF_1 and BUF_2 to the input of PRE_1. Both subtractors are disabled when the ground potential is passed through them, so they merely act as S&H circuits. Once the ground potential has reached PRE_1, the precision gain amplifier is reconfigured as a unity gain amplifier by setting the appropriate switches. At this point the procedure can be altered depending on the accuracy desired. All methods reproduce a value at the output of PRE_1, which is the stage's offset voltage, at the point used for the offset voltage subtractor.

Gain errors can be corrected by setting BUF_1's or BUF_2's or PRE_1's input to $V_{REF}/2^s$. The reason for skipping over BUF_1 is that the correction of BUF_1's gain error may add more error than it corrects. That is, when the precision gain circuit compensates for BUF_1's gain error, it modifies the DAC's subtracted voltage. It is also possible that by including BUF_1 in the gain calibration the subtrahend reduced by λ will be restored closer to its correct value. Similarly BUF_2 may also be skipped over and then the offset voltage reduction procedure will be unmodified as well. For all input paths the signal is passed to the input of PRE_1 with only the offset voltage cancellation being performed. The calibration procedure then continues as previously explained in the chapter devoted to the circuit.

The high gain/low offset op-amp used for the precision gain calibration procedure can have its offset voltage reduced when a valid sample is at PRE_1's input. This is a point in the conversion sequence that does not require the use of PRE_1. It may also have its offset reduction performed when the stage's offset voltage is being measured, if the high gain/low offset op-amp is not used in the procedure.

5.4 NORMAL OPERATION

All full stages perform the same operations but they do not all occur coincidingly. To understand the sequence of events that occurs during the analog to digital conversion, the first two stages of an arbitrary sized ADC will be examined. It is not important which procedure is first, only the order of occurrence is. It is also important to realize that the proposed converter's full stage can work on two independent inputs by isolating them from each other by opening either SW_1 or SW_2. To demonstrate this, the voltage offset reduction procedure will be explain in greater detail for this explanation of the full stage's normal operation. However the precision gain calibration phase will not be elaborated upon as much, because the explanations on pipelining can be carried over from the offset voltage reduction discussion. To aid in this discussion, table 5.1 is included to indicate which process is being performed at the inputs of an arbitrary full stage's amplifiers. The processes being considered are: offset reduction (V_{os}), gain calibration (gain), and sample conversion (samp). Only three adjacent full stages are shown in the table, but this information should be adequate to follow the sequences in all the stages.

The offset voltage reduction procedure begins by setting the input of BUF_1 to the ground potential. After BUF_1's output has settled SW_1 is closed, but it is later opened once BUF_2's output voltage has settled. Then from BUF_2's input onward the offset voltage reduction procedure continues. Just before SW_1's opening and immediately after, C_1's bottom plate is held at ground potential. Therefore, no signal corruption occurs due to the switching of C_1's bottom plate. The subtractor used to subtract the recorded offset voltage is also disabled.

A valid sample is then placed at BUF_1's input. The internal ADC can now begin to digitize the sample. At this point the sample is isolated from the accumulated offset voltages by SW_1. Next SW_2 is opened, SW_1 is closed and PRE_1 is reconfigured as a unity gain amplifier. The reason for the reconfiguration of PRE_1 is that the measured offset voltage is subtracted before PRE_1's output. Therefore, the accumulated offset must be measured up to PRE_1's input. This requires a unity gain amplifier if the voltage is to be measured at the stage's output. With the sample still being held at BUF_1's input, the stage's offset is recorded. The valid sample and offset voltage are isolated from each other

Table 5.1 Full stage process sequences

	STAGE x			**STAGE x+1**			**STAGE x+2**		
TIME	**BUF**$_1$	**BUF**$_2$	**PRE**$_1$	**BUF**$_1$	**BUF**$_2$	**PRE**$_1$	**BUF**$_1$	**BUF**$_2$	**PRE**$_1$
1	samp	V_{os}	V_{os}	V_{os}	samp	samp	samp	V_{os}	V_{os}
2	samp	samp	V_{os}	V_{os}	V_{os}	samp	samp	samp	V_{os}
3	gain	samp	samp	samp	V_{os}	V_{os}	gain	samp	samp
4	gain	gain	samp	samp	samp	V_{os}	gain	gain	samp
5	samp	gain	gain	gain	samp	samp	samp	gain	gain
6	samp	samp	gain	gain	gain	samp	samp	samp	gain
7	V_{os}	samp	samp	samp	gain	gain	V_{os}	samp	samp
8	V_{os}	V_{os}	samp	samp	samp	gain	V_{os}	V_{os}	samp

by SW_2. After the offset voltage has been recorded at the stage's output and BUF_2's output has stabilized, SW_1 is opened and SW_2 is closed. The internal DAC's converted voltage is then connected to the subtractor to begin the first phase of subtracting the converted voltage from the sample. In the second phase of the subtraction SW_1 is opened and SW_3 is connected to the ground potential. This produces the required difference signal at BUF_2's output, which is then connected to PRE_1's input. The stage's input is in turn connected to the precision gain calibration voltage, while the precision gain circuit amplifies the input sample. For this procedure PRE_1 is set to have a gain of 2^s. Isolation of the two separate values is again provided by SW_1.

During the precision gain calibration phase the calibration voltage is passed through the stage as described previously. At this point the second stage has a valid processed sample at its input. The sample will proceed in the same manner as the original sample had in the first stage. Just prior to the first stage producing the valid processed sample at its output, the first stage's offset voltage was set at its output. During this time interval, the second stage could be starting one of its error correction procedures. Going back one more processing step, to when the first stage's offset voltage reduction procedure was just being initiated, the second stage would be initiating its sample processing mode whether a valid sample was present or not.

The explanation now returns again to the converter's present state; as a recap, the precision gain calibration is just starting in the first stage. During the second phase of the procedure the first stage's input is connected to another valid sample. The sample is isolated from the gain calibration voltage by SW_1. Also during this phase, stage two can now begin its other error correcting procedure, because stage one has the processed precision gain calibration voltage at its output.

With this method of error correction the digital control signals driving the switches of the first stage can be delayed τ seconds (one maximum stage delay), and then used to drive the second stage's switches. Only one such digital delay system is required because the first stage's switch control signals can be used to drive every other full stage, while the delayed switching signals can drive every other full stage starting with the second full stage.

As a result of correcting alternate error sources between valid samples the effective sample rate of the proposed converter is reduced by a factor of two when compared to the standard pipelined algoritmic architecture.

5

6. SIMULATIONS OF THE PROPOSED CONVERTER AND ITS FLEXIBILITY

This chapter will provide information on how to obtain the parameters for the maximum wordlength simulation. These values, of course, are mainly for illustrative purposes because many of the required process parameters are not released to the University. The values chosen for the simulation are meant to be as close as possible to what can be expected from the Northern Telecom CMOS 1B 5μ process. Process parameters that were available were used [CMC,1984]. In the second part of this chapter some suggestions are made on how to modify the proposed converter to produce alternatives in the conversion characteristic, speed, and die area used.

6.1 SPICE SIMULATIONS

The circuit simulation package used to provide the results given for the analog circuitry designed was SPICE version 2G.6 [VLADIMIRESCU,1981]. Several problems and/or errors resulted when using the package, either because of software bugs or its implementation on the University's VAX. These problems included:

1. Small differences in results obtained using the same data on different occasions.
2. Nonconvergence of operating point information, even when convergence occurred on a previous DC simulation including the operating point within the same file.

3. Nonconvergence of DC and TRAN (transient) analysis until a bogus element or device is constructed to counteract the problem.
4. Nonconvergence of data in all simulations after a geometry change or after a compensation network has been added, even if the simulation converged on the previous run.
5. Nonconvergence of data in all simulations for unknown reasons.

For these reasons the data provided by the included simulations, especially for transient analysis, will be considered about 90% accurate. When a DC analysis does provide data, it is usually correct and is deemed to be the most valid simulation, as it can be verified using hand calculations. As a result of the nonconvergence problems the circuits simulated could not be optimized. This becomes a severe problem when trying to compensate a circuit. Therefore, the simulation runs that did converge were used to determine trends in the data to arrive at the specifications given.

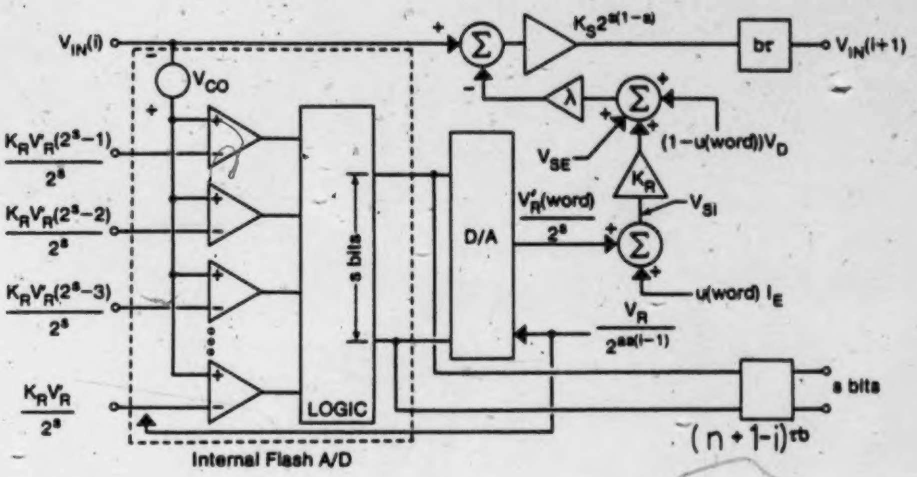
6.2 INPUT PARAMETER CALCULATIONS

When using the software included in appendix one, designers must provide their own input parameters. The parameters for the proposed ADC will be calculated using the realization detailed in the previous chapter (figure 5.1) and results demonstrated within this thesis. Therefore, if the precision gain circuits calibration voltage is set at any point other than BUF_1's input the expressions for K_S, V_{SE} and V_{SI} will be altered. The expressions will have their values changed by some multiple of the buffer amplifier's gain A_{BUF}. Note also that each stage's input would also be affected. That is, V_{IN} for this simulation would be modified the same as the above expressions will, as detailed in the following account. When BUF_1 is skipped over in the precision gain calibration phase, each of the affected equations is multiplied by A_{BUF}. If BUF_2 is skipped over as well, the equations used when BUF_1 was skipped over may be used once they have been multiplied by A_{BUF}. To aid in this discussion on how to calculate the various error values the diagram that illustrates these is repeated in figure 6.1. For a formal explanation on how the values contained within the following formulae are obtained refer to the referenced or implied chapter.

The stage gain errors K_S, K_R, and λ are considered first. By using the precision gain circuit the stage's gain error K_S is primarily given by the precision gain circuit's accuracy. Therefore,

$$K_S = \frac{A_{OL}(1+V_{OS}/V_{REF})}{(1+A_{OL})(V_{SE}/V_{REF}2^s+1)} \qquad (6.1)$$

This formula is broken down further during the simulation. All the s independent quantities are grouped in:


$V_{IN}(i)$
V_{CO}
$\frac{K_R V_R(2^s-1)}{2^s}$
$\frac{K_R V_R(2^s-2)}{2^s}$
$\frac{K_R V_R(2^s-3)}{2^s}$
$\frac{K_R V_R}{2^s}$
LOGIC
s bits
Internal Flash A/D
D/A
$\frac{V_R'(word)}{2^s}$
$\frac{V_R}{2^{as(i-1)}}$
$K_S 2^{a(1-s)}$
br
$V_{IN}(i+1)$
λ
V_{SE}
$(1-u(word))V_D$
K_R
V_{SI}
u(word) I_E
s bits
(n+1-i)th

a=1 -flash converter b=1 -pipelined version
a=0 -algorithmic converter b=0 -cascade version

$u(x)=0$; $x=0$ $V_R'=V_R/2^{as(i-1)}$
$u(x)=1$; $x>0$

V_R - the converter's reference voltage

V_{CO} - maximum comparator offset error

K_S - stage's gain coefficient ($K_S=1$)

V_{SE} - various internal error offset voltages

V_D - used to change the error when the digital output of the stage is zero

V_{SI} - the ideal D/A output summed with V_R dependent quantities

I_E - integral linearity error of the D/A

word- the numerical value of the D/A's output ($0 \leq word \leq 2^s-1$)

K_R - stage's reference voltage coefficient ($K_R=1$)

λ - subtractor's gain coefficient ($\lambda=1$)

Figure 6.1 Full stage of an algorithmic or series-flash converter with either cascade or pipeline architecture.

$$K_{SP}= \frac{A_{OL}}{(1+A_{OL})}(1+V_{os}/V_{REF}) \qquad (6.2)$$

which is entered as an input parameter, while the remaining s dependent term is evaluated within the program. The reference voltage's gain coefficient K_R is determined by the off chip reference. With trimming, approximately 16 bits accuracy should be obtained [GREBENE,1984]. This gives

$$K_R= \frac{2^{16}-1}{2^{16}} \qquad (6.3)$$

The subtractor's gain error λ is given by

$$\lambda= \frac{1}{1+C/C_p} \qquad (6.4)$$

Next, stage offset voltages V_{CO}, V_{SE}, V_D and V_{CN} are considered. The internal ADC's comparator offset voltage V_{CO} is given by

$$V_{CO}= \frac{V_{TOG}}{A_{OL}} \qquad (6.5)$$

where V_{TOG} is the toggle voltage necessary to produce a binary one, and A_{OL} is the comparator's gain. The various internal, voltage reference independent, offset voltages are grouped in the term V_{SE} which is given by

$$V_{SE}= [\Sigma V_{os}-\lambda(\Sigma V_{os}+V_{ros})]/A^2_{BUF} \qquad (6.6)$$

where ΣV_{os} is the sum of BUF_1, BUF_2, and PRE_1's offset voltages, and V_{ros} is the offset voltage introduced during the stage offset measurement procedure. The V_D voltage reduction is not required for the proposed converter because of the way the internal DAC is implemented. By combining the normalized comparator offset voltage and voltage reference's error the partial stage's maximum offset error can be formed by:

$$V_{CN} = V_{CO}/V_{REF} + |1-K_R| \tag{6.7}$$

The last two quantities to be considered are V_{SI} and I_E which are the ideal DAC output voltage summed with voltage reference dependent quantities and the DAC's integral linearity error, respectively. Again because of the fashion in which the internal DAC's voltage is generated the error portion of V_{SI} is reduced. Therefore,

$$V_{SI} = [V_{REF}\frac{word}{2^{c(i-1)a+c}} + I_E]/A_{BUF} \tag{6.8}$$

where *word* is the digital output produced by the internal ADC, and c is the number of bits determined in the stage. The I_E has the value of the maximum difference between the actual voltage reference fraction and its ideal value. This can give a maximum value of

$$I_E = V_{REF}|1-1/K_R| \tag{6.9}$$

This error has been divided by K_R so that it can be included in the V_{SI} term, which is multiplied later by K_R.

The above formulae are used with information obtained in other chapters to arrive at the following table (table 6.1) of values. Some of the values used to determine the parameters are included in the next table (table 6.2).

6.3 MAXIMUM WORDLENGTH SIMULATION

Using the parameters given in table 6.1 the maximum wordlength simulation program can be used to give an approximate value for N. The table that follows (table 6.3) indicates how various combinations of s and r produce an N. The resulting maximum conversion error is also reported.

To provide a better view of the conversion errors, several graphs were formed that indicate the conversion error on the y axis, and the input voltage that produced the error on the x axis. The stage simulation program was used to produce the values. Only 4 increments were used in between adjacent quantization levels. This causes the graphs to appear nonsymmetric. The reason for this is that the routine that was used to graph the data only does linear extrapolation between adjacent points. Therefore, because there are not enough data points to produce all conversion error greater than roughly |0.25| LSBs, the graphs produced appear to indicate less conversion error than is actually present. The graphs however still provide useful information. That is, a comparison of various combinations

Table 6.1 The proposed converter's internal error values

ERROR NAME	ERROR VALUE	UNITS
K_S[†]	1.0012 to 1.004	
K_{SP}	1.0002341	
K_R	0.9999847	
λ	0.99900	
V_{CO}	3.5	mV
V_{SE}	-0.930712	mV
V_{CN}	0.001765	
I_E[‡]	30.6	μV

[†] range indicated for s=1 and s=3

[‡] the actual value is shown here

Table 6.2 Parameters required for error value calculations

PARAMETER	**VALUE**	**UNIT**
C/C_p	0.001	
V_{ros}	1.0	mV
V_{REF}	2.0	V
V_{tog}	2.5	V
A_{OL}(comp.)	96	dB
A_{BUF}	0.998	
A_{OL}(equiv. buff.)	500	
V_{os}(low offset op-amp)	0.5	mV
V_{os}(buff.)	24	mV
V_{os}(prec.)	24	mV

Table 6.3 Maximum wordlength combinations

s	r	N	MAXIMUM CONVERSION ERROR (LSB)
1	1	6	0.50
1	1	7	0.63
1	1	8	0.88
1	1	9	1.00
2	2	6	0.50
2	1	7	0.50
2	2	8	0.88
2	1	9	1.00
3	3	6	0.50
3	1	7	0.50
3	2	8	0.88
3	3	9	0.90

of stage wordlengths producing the same N can be studied to see which produces a characteristic closest to the ideal version.

In figure 6.2(a) an ideal characteristic is shown for an 8 bit ADC producing 2 bit per full stage and 2 bits in the partial stage. An expanded view of what is being plotted is shown in figure 6.2(b). This figure shows two adjacent quantization levels and the error produced during an ideal conversion in between these points. Part (b) of the figure also shows what portion of the ideal graph is being plotted in figure 6.2(a). Graphs of ideal conversion for other values of s, r and N have the same appearance (INC=4) as figure 6.2(a). The only dissimilarity in the graphs would be that a different number of points would be plotted.

Graphs for the proposed ADC with the same plotted precision produced using s=1, 2, and 3 bits are indicated in figures 6.3 through 6.5. From these graphs it can be seen that the lowest number of conversion errors greater than what occurs in the ideal graphed data is produced by the converter using s=2 bits. The converter that produces the most conversion errors greater than 0.5 LSBs is formed using s=1 bits.

Another point worth noting is that there is a major transition in the plot produced when simulating the proposed converter for s=1 bit. The transition occurs very close to the point where the first full stage of the converter must subtract its bit's voltage equivalent from the input during

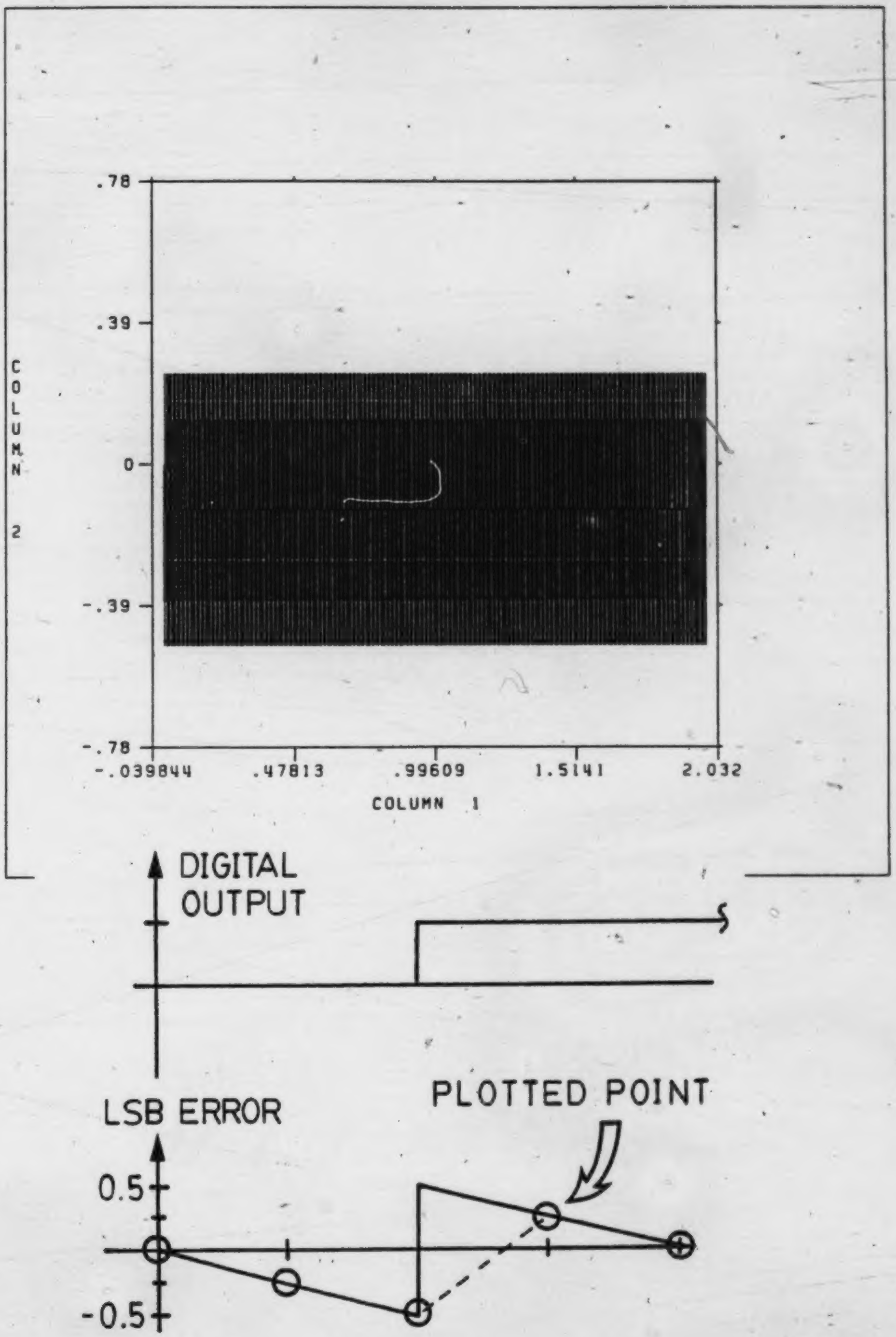


Figure 6.2 (a) Scatter plot of conversion error for an ideal conversion with N=8 s=r=2 and inc=4; (b) expanded view of one plotted quantization step

processing. This suggests that it may be worth while investigating the effect of distributing stage errors. That is, by forcing the first stage or stages in the proposed converter to produce less error than the following stages there may be a substantial increase in the bits produced. The reason this seems logical is that small error changes in the first stage, due to a bit pattern change in the stage, seem to produce the converter's maximum conversion errors. This assumption is supported further by the other two plots. In these plots there are spikes of the maximum conversion error at points where bits in the ADC's first stage change.

In order to determine which of the two main error groups produces the most conversion errors, the stage simulation program was run with one of the groups set to their ideal values. That is, one of the data groups was left at the value used to simulate a practical ADC while the other group was set to the values used during the ideal conversion simulation. Figure 6.6 shows the graph produced when the stage gain coefficients were made ideal (K=1), while figure 6.7 is a graph generated using the ideal offset voltage values (V_{os}=0).

A comparison of the graphs yields two significant points about the proposed converter. The first most notable point is that reducing the stage offset voltages reduces the recorded frequency of conversion errors larger than 0.5 LSB to zero. Running the maximum wordlength simulation program also indicates an offset reduction can increase the

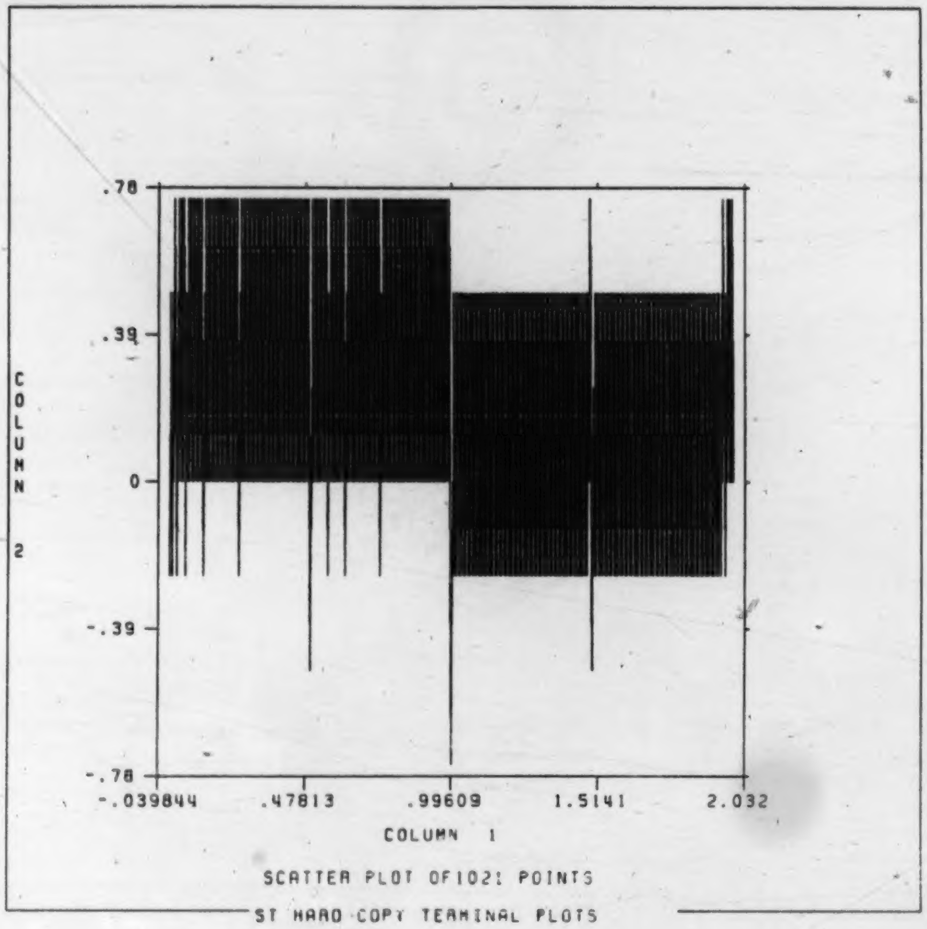


Figure 6.3 Scatter plot of conversion errors for the proposed ADC with N=8 and s=r=1

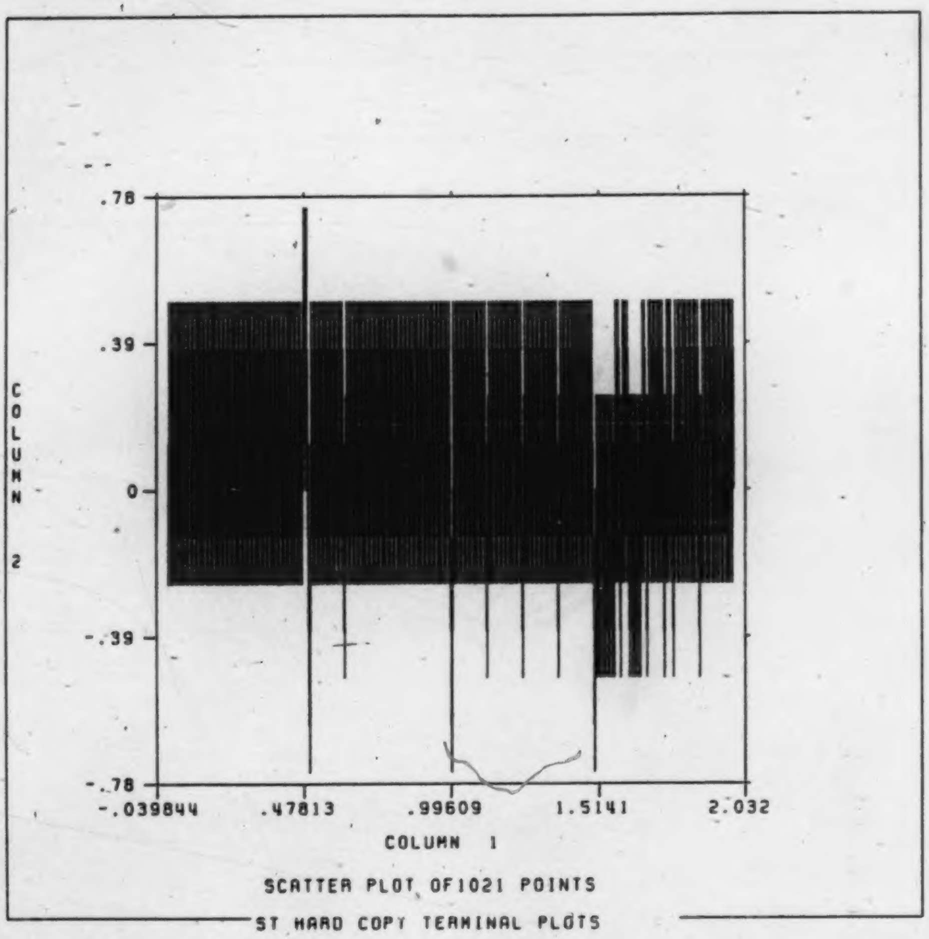


Figure 6.4 Scatter plot of conversion errors for the proposed ADC with N=8 and s=r=2

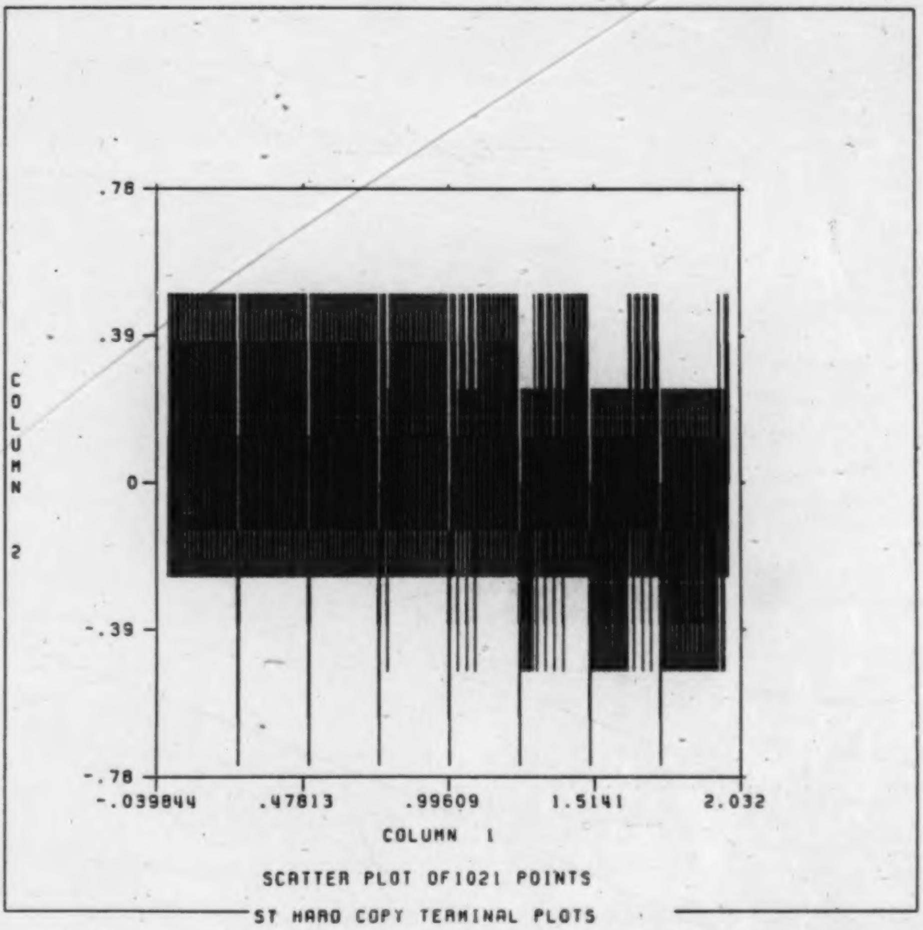


Figure 6.5 Scatter plot of conversion errors for the proposed ADC with N=8 and s=3 r=2

wordlength produced. It should also be realized that the stage's offset voltages will affect the stage gain coefficient K_S for the proposed architecture. The other information obtained from the comparison is that reduction of the gain errors can increase the frequency of conversion errors larger than 0.5 LSB. This indicates that stage gain errors can tend to partially cancel other error sources. Moreover, this may also indicate that a worst case analysis did not occur when using the parameter set chosen for the simulation. Figure 6.6 also has its maximum conversion errors occur around input values that correspond to changes in the first and second stage's bits.

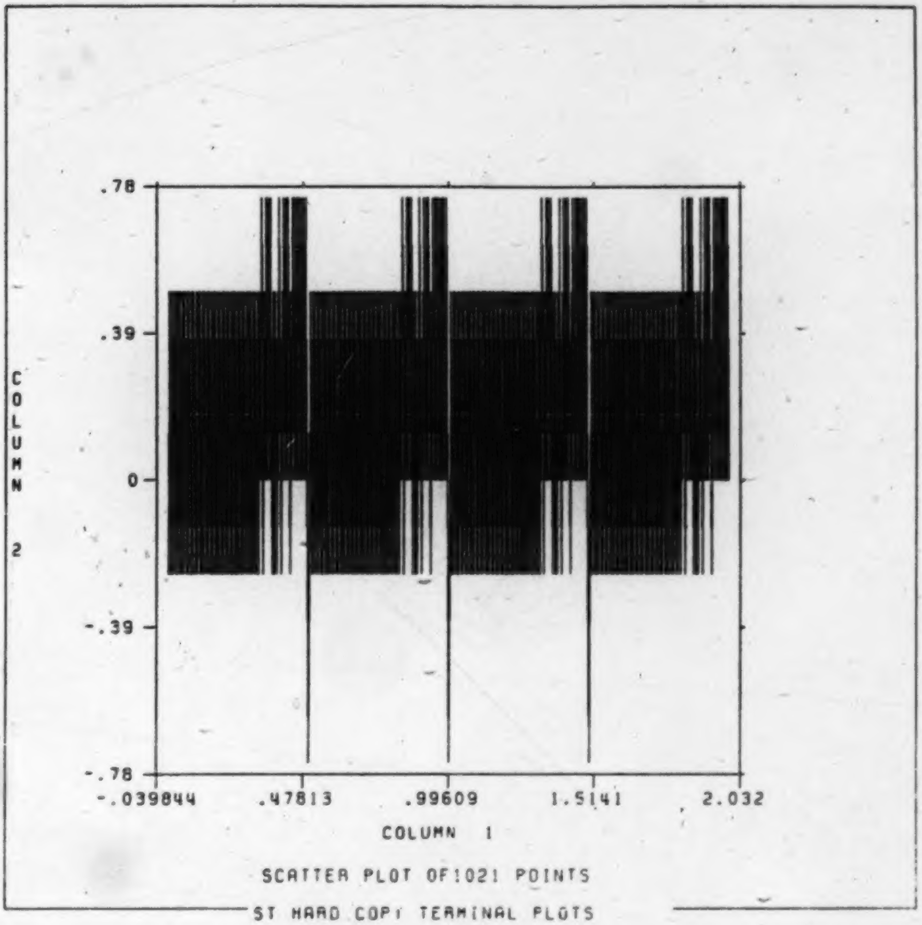


Figure 6.6 Scatter plot of conversion errors with ideal values of gain coefficients, and with N=8 s=r=2

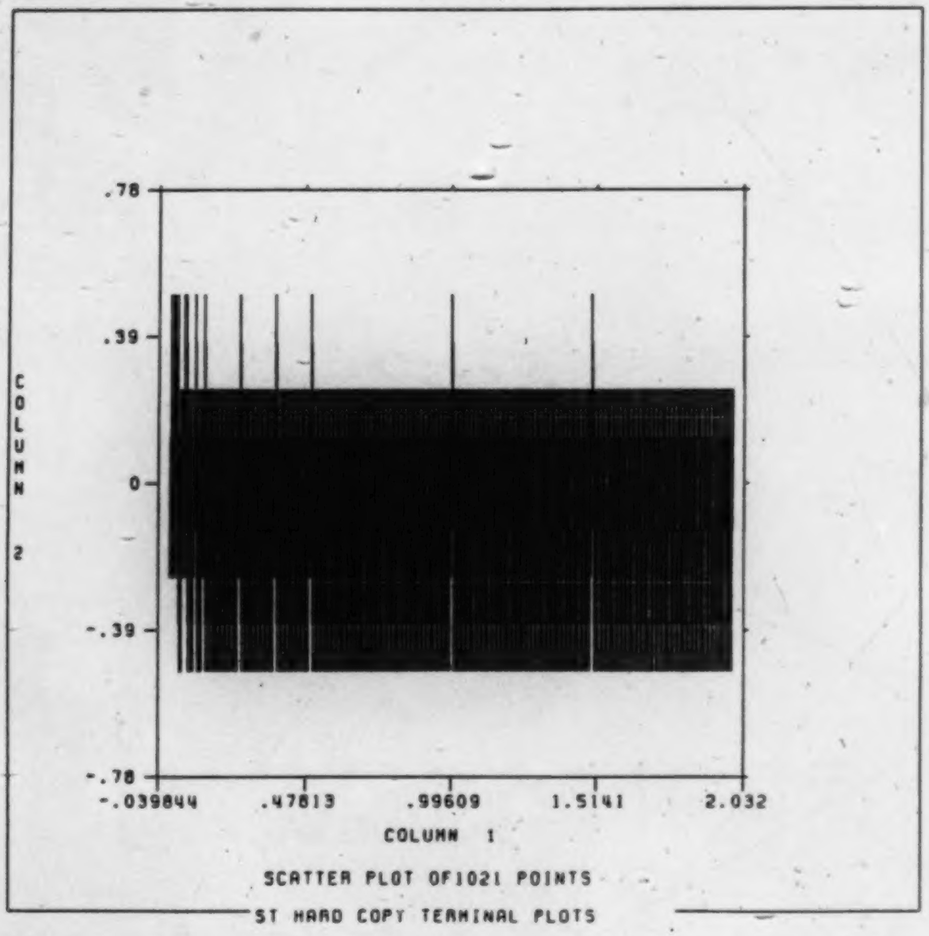


Figure 6.7 Scatter plot of conversion errors with no offset voltages, and with N=8 s=r=2

6.4 THE PROPOSED CONVERTER'S FLEXIBILITY

Several features of the proposed ADC's architecture make its conversion characteristic flexible. The segmented structure of the device makes it possible to increase the resolution by inserting full stages. For each full stage inserted, s additional bits are produced. This process of adding additional full stages is limited by the error tolerances of the stages used. A second benefit of the segmented structure is that once a full stage has been laid out, all the other full stages are identical and the same layout may be used. Furthermore, the partial stage is a reduced version of the full stage which consists of just the internal flash converter. Therefore, the full stage's layout could be reduced to just the internal flash converter to yield the partial stage's layout. The benefits of this are many. Designers may now prototype a design using a small wordlength, and then increase the precision after various other on chip devices are functional. This contrasts with the other possibility of either working on the analog and digital circuits separately and then combining them on a chip; or providing two unique ADCs, one for the first test phase and one for the second. The proposed ADC also greatly facilitates both design and process improvements, if the goal is to increase the precision of the converted information without selecting a new architecture.

The wordlength of the proposed ADC can be increased once it is at its maximum as governed by the stage error tolerances, by making a trade-off with other converter specifications. In all cases the stage errors are reduced, and hence the new maximum wordlength can be made larger than its previous value. By reducing the conversion rate, or by increasing the amount of error correction hardware, the errors will be reduced. Therefore, the conversion rate or die area can be traded off against the precision produced.

To produce a nonlinear conversion characteristic with the proposed converter, the precision gain circuit and the subtractor circuit can be combined with some additional analog and logic circuits. The same segmented structure can be used for NADC applications. Most of the architecture modifications would be on how the reference voltages were generated. To understand this, recall that most NADCs have a segmented structure [GREBENE,1984]. The segments are then broken down linearly. At present the proposed ADC performs linear quantization. Therefore, if the segment that the input lies within is identified, the following conversion is linear and may be performed by the present converter architecture.

The segment that the analog input is within could be identified by the first stage of the NADC. This stage would be modelled after the full stage structure, but it would have to produce $\log_2$[segments] bits, and it would only have a unity stage gain. This stage will be referred to as the nonlinear stage. A logic network connected to this stage would then set the voltage references to be used in all of the following stages, where only linear conversion is required. Once the nonlinear stage has identified the segment where the input lies, the input would have the voltage given by the lower bound of the located segment subtracted from it. The following linear conversion would use the difference between the upper and lower determined segment voltages as V_{REF}. To produce the voltage references required, a combination of precision gain stages and subtractor circuits might be used.

If the die area taken up by the converter is considered to be the priority in a project, the conversion may be performed by recirculating the processed input. Only full stages would be used, and the number of them required would be given by

$$n= \frac{N}{T_R s} \qquad (6.10)$$

where T_R is the number of times the processed input is processed by the n full stages. To do this, the last full stage's expansion output would be redirected back to the first stage's input T_R times. A switch at the first stage's input would connect either a new sample or a partially processed sample to the stage. After an

$$\text{initial delay}= n\tau T_R \qquad (6.11)$$

a digital output is made available every

$$\text{delay}= \tau T_R \qquad (6.12)$$

seconds. This would reduce the die area required by approximately T_R times for the case when $r=s$. The maximum processing delay is increased by the same amount T_R.

7. CONCLUSION

This thesis presented an investigation and development of a pipelined algorithmic converter architecture. The proposed ADC has a segmented structure that provides *s* bits of information at every stage but the last, which produces *r* bits. A digital CMOS technology can be used to fabricate the proposed ADC, because on chip error correction reduces the problems inherent to the process used. To provide precise voltage references, the use of external sources is suggested. This should produce larger wordlengths and result in higher yields than would be possible if the voltage references were also produced on chip.

An error analysis was performed on both the serial-flash and algorithmic converters. The analysis provided equations that revealed how the various error sources considered contribute to conversion errors. This was done for two extremes in the analog input (lowest and highest quantization levels). Results obtained when using these formulae indicated that the worst case conversion errors vary with the input's value and with stage parameters.

In order to estimate the worst case conversion error with a higher accuracy, a stage simulation program was developed. This program enables the user to simulate conversion of all the possible quantization levels, including intermediate values if desired. Then using this program a second simulation program was formed that would arrive at an estimate of the maximum wordlength for the chosen ADC architecture (series-flash or algorithmic) and parameter set. The second program provides the maximum wordlength estimate for different values of s until the specified conversion error has been reached.

A third program was developed to simulate an ideal version of the proposed converter. This was done to provide information on the maximum permissible offset voltage errors for all the comparators used within the converter. The program verifies theoretical calculations made on the error tolerances of the comparators.

To provide rapid conversion at low power consumption levels a specialized buffer amplifier was developed. Simulations of the buffer indicate it will provide a higher slew rate at lower bias levels than a general purpose amplifier configured as a unity gain buffer. The buffer uses a unique open loop design to produce its high slew rate. Several innovative features are employed in the buffer's design. Both the buffer and its features could be used for other circuit designs.

An electronically calibrated precision gain circuit was designed to produce a high accuracy stage gain using a digital process. This device could also be used in other circuits that only have low tolerance resistors available, but still require a precise gain independent of the resistor tolerance. The precision gain circuit is not restricted to CMOS technology because a JFET can be substituted for the

NMOS transistor used in the circuit.

Using the maximum wordlength simulation program with the data obtained on the various internal circuits it appears that the proposed converter should be able to produce 8 bits precision with less than 1 LSB conversion error. The best combination of full stage wordlength and the partial stage's wordlength is process parameter and precision dependent.

7.1 FUTURE CONSIDERATIONS

The first area worth considering, that would be useful in any future research, is determining how stage error distribution effects conversion errors. Then continue by permitting a variable number of bits to be determined in each stage. This may lead to an architecture modification that would increase the obtainable precision.

Both the buffer and precision gain circuits should be fabricated and have their performance checked. The simulations of these devices indicate they are feasible, but the fabricated devices would provide additional information on the required sizes of important transistor pairs and other process limitations. If large capacitive loads are to be driven (above 1 pF) using the buffer, some internal compensation is necessary. Preliminary work suggests that a resistor and capacitor in series between the buffer's output and the gate of M_5 is a feasible means of compensation. The effect of varying the substrate bias of the buffer amplifier should be investigated further, when a new simulation package is available. Reducing the substrate bias would increase the buffer's frequency response as indicated by some of the theoretical calculations made. It may also be advisable to look into some buffer architecture changes. For example, some of the critical current sources could be replaced by more elaborate higher impedance current sources. Before the circuits are fabricated, they should be resimulated using a working (more reliable) simulation package. The circuits should also be optimized for the process being used.

Another concern is for the proposed converter's chip layout. Particular attention should be placed on how the voltage references are passed to the stages. That is, how much decoupling and isolation from the adjacent digital circuitry is necessary to make the references useful.

On chip reference voltage generation should be explored more fully. That is, switch capacitor digital to analog conversion circuitry could be used to generate fractions of an input voltage reference. This would reduce the external circuitry and the IC pins required. To provide nonlinear conversion a logic network and analog reference generating circuit is necessary. Both these circuits have yet to be investigated. The use of the previously designed subtractor and precision gain circuitry is suggested.

To reduce device offset errors the use of AC coupling for the low order bits should be investigated. This should increase the obtainable precision if the low order bits vary at a suitable frequency above zero hertz.

7.2 THE PROPOSED ADC'S FEATURES AND POSSIBLE APPLICATIONS

Before discussing suitable applications for the proposed converter, its estimated performance specifications will be detailed. The estimated and/or simulated values, and some of the ADC's features are:

1. 6 to 8 bits resolution at s=1 to s=3 bits
2. 200KHz to 700KHz sample rate
3. less than 1 LSB conversion error
4. ±1/2 LSB differential linearity error (no missing codes)[†]
5. no sample and hold amplifier is required
6. low power requirement (approximately less than 200 mW)
7. majority of the chip may be fabricated using a digital CMOS process
8. low environment dependence due to on chip error correction
9. the precision is readily modified by altering the number of stages
10. a change in the ADC's precision does not affect the effective sample rate
11. the precision may be increased by increasing the die area used for the error correction and/or by reducing the conversion rate

12. the die area required by the converter can be reduced by recycling the processed data
13. nonlinear conversion is possible
14. low supply voltages (±5 volts)

† This value can be more reliably determined once several full stages have been fabricated and tested, because it is process and device size dependent.

The medium speed operation of the proposed ADC limits the sampled input frequencies to below 350KHz in the best case. This tied in with the produced wordlengths size, and the low environment dependence make the ADC suitable for the following applications:

1. Automobile control systems
2. Sensor, microprocessor and ADC single chip integration
3. Biomedical circuits for implant, where device size and power consumption are important
4. Multiplexed low fidelity audio applications (approximately 80 channels per device)
5. Outdoor instrumentation

This investigation has led to results that indicate that the proposed converter is worth investigating further. Only after additional research will a viable ADC be possible.

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APPENDIX ONE

This appendix includes three programs that were discussed in chapter 2. The comments within the programs should be clear enough without further explanation. All the programs have been test on MS-DOS and UNIX systems. Therefore, they should be readily transported to most computer systems without modification.

```
/* This program is used to calculate the maximum tolerable comparator
 * error for an ideal converter. As such, the maximum value to be
 * dealt with is 1/2 LSB . Hence, this program performs its calculations
 * in 1/2 LSBs using integers to represent all values. This proceedure
 * eliminates round-off error.
 */

#include <stdio.h>
main()
{
  int n,s,r,stages,ampf,refmax,refmaxp,maxv[63],vcom,delta,vin,k;
  int compcont,pcomp,i,ampp,t;
  int power();

/* data entry */
  printf("enter a value for N:\n");
  scanf("%d",&n); /* the number of bits 'n' to be converted */
  while( n > 10 )
  {
     printf(" N values are less than or equal to 10 only !\n");
     scanf("%d",&n);
  }
  printf("enter a value for s:\n");
  scanf("%d",&s); /* the number of bits s determined in a full stage */
  while( s > n )
  {
     printf(" s values must be less than N !\n");
     scanf("%d",&s);
  }

/* constant calculations */
  r= n % s;     /* the number of bits r determined in the last stage */
  if(r == 0)
    r=s;  /*  if N is an integer multiple of s then set r=s  */
  stages= (n-r)/s; /* number of full stages */
  k= power(2,n+1);  /* number of 1/2 LSBs to full scale */
  ampf= power(2,s); /* amplification value of the full stage */
  refmax= (ampf-1)*k/ampf;  /*  max quantization level in the full stages in 1/2 LSBs */
  ampp= power(2,r);
  refmaxp= (ampp-1)*k/ampp;  /* max quantization level in the partial stage in 1/2 LSBs */
  compcont= (ampf-1)*stages + ampp-1;  /* number of comparators in the entire converter */

/* array initialization */
  for(i=0;i<=61;maxv[i]=1024,i++)
  ; /* initialize array to the max error for 10 bits  */

/* create all the possible quantization levels */
/*  working in 1/2 LSBs  */
```

```
  for(t= 1; t<=k : t +=2)
  {
    vin=t;  /* pass on the new value of vin */

/* simulation of i full stages */
        for(i=1; i<=stages; i++)
          {

/*  simulate single full stage */
                  for(vcom=refmax; vcom>0; vcom -= k/ampf)
                  {
/* generate all the reference levels, and compare to the input until vin is located */
/* start at the highest reference level and work down */
                    delta=vin-vcom;  /* find the separation between vin and the reference level being checked */
                    delta=abs(delta);
                    pcomp=compcont-(ampf-1)*(stages-i)-(ampp-1)-vcom*ampf/k;  /* present comarator being checked */
                    maxv[pcomp]= min(maxv[pcomp],delta);  /* save smallest separation */
                          if(vcom<vin)
                            {
                                  if(vcom == k/ampf)
                                    ;  /* no lower comparision can be made */
                                  else
                                  {
                                    delta= vin-vcom+k/ampf;  /* find separation between vin and the next lower reference level
                                    * once it has been estabilished what reference value vin is just below */
                                    delta=abs(delta);
                                    pcomp=compcont-(ampf-1)*(stages-i)-ampp+1-vcom*ampf/k+1;
                                    /* comparator after the comparator being checked */
                                    maxv[pcomp]= min(maxv[pcomp],delta);  /* save smallest separation */
                                  }
                                    vin -= vcom;  /* subtract the reference voltage that vin is just below  */
                                    vcom= k/ampf;  /* results in search termination of the full stage  */
                            }  /* continue search */
                  }  /*  end of full stage simulation  */
                    vin *= ampf;  /* amplified the processed input by the stages gain prior to pasing it to the next */
          }  /* end of all full stages  */

  /*  partial stage simulation follows  */
  for(vcom=refmaxp; vcom>0; vcom -= k/ampp)
  {
  /* again compare vin to the reference levels starting at the highest */
    delta=vin-vcom;  /* find the separation between vin and the reference level being checked */
    delta=abs(delta);
    pcomp=compcont-vcom*ampp/k;  /* present comparator being checked */
    maxv[pcomp]= min(maxv[pcomp],delta);  /* save smallest separation */
          if(vcom<vin)
          {
                  if(vcom == k/ampf)
```

```
                        ; /* no lower comparision is made  */
                       else
                       {
                         delta= vin-vcom+k/ampf;  /*  find the separation between vin and the next lowest reference level  */
                         /* once it has been established what reference value vin is just below */
                         delta= abs(delta);
                         pcomp= compcont-vcom*ampp/k+1;  /* present comarator being checked + 1 */
                         maxv[pcomp]= min(maxv[pcomp],delta);  /* save smallest separation */
                       }
                         vcom= k/ampp;  /* insures termination of the full stage search */
                 }
        }  /* end of partial stage simulation  */
  }  /* end of the converter simulation */

  printf(" N=%2d, s=%2d, r=%2d\n",n,s,r);
  for(i=0; i<compcont; i++)
  {
    if(i % (ampf-1) == 0)
      printf("----------  new stage  ---------\n");  /* stage separator  */
  printf(" comparator %2d, error max in 1/2 LSBs is %10d\n",i+1,maxv[i]);
   }  /* end of print out */
}  /* end of main  */

/* functions */


/*  base raised to the power of exp, both are positive int  */
int power(base,exp)
int base,exp;
{
  int value;
  for(value=1; exp>0; value *= base, exp-- )
  ;
  return(value);
}  /* end of program */
```

```
/* THIS PROGRAM 'SIM' IS USED TO SIMULATE A COMPLETE CONVERTER
 * EITHER THE ALGORITHMIC OR SERIAL-FLASH CONVERTER.
 * TO PRODUCE DATA ONLY USE THE -D OR -d SWITCH THIS WILL
 * PLACE A * IN THE FIRST COLUMN AT MAXIMUM VALUE PRINT OUTS
 * A -M OR -m SWITCH MAY BE USED TO PRODUCE ONLY THE MAXIMUM ERROR VALUE.
 * BOTH SWITCHES MAY BE USED TOGETHER IF SEPARATED BY AT LEAST ONE SPACE.
 */

#define YES 1
#define NO 0
#define SMAX 3
#define IMAX 12
#define abs(x) (((x)>0)?(x):-(x))

float vin,veq,vr,vse,vd,vco,kr,ks,lam,ie,abuf;
int a,dflag,mflag,loc;

main(argc,argv)
int argc;
char *argv[];

{
        extern  int a,dflag,mflag,loc;
        extern  float vr,vse,vd,vco,kr;
        extern  float ks,lam,ie,abuf;
        int n,s,inc,kpoint,first;
        float mperr,ksp;
        float sim();

        /* INPUT VALUES
         * n    s     inc
         * vr   vco   vse   vd
         * kr   ksp   lam   abuf
         * a
         * kpoint
         * mperr (IGNORED VALUE, BUT MUST BE PRESENT)
         * loc
         *
         * A check for the correct number of data elements is made
         * and the inc size is checked to insure that no more than 12 steps (IMAX) are used
         * and that it is not to small.
         * Parameter 's' is checked as to its validity.
         * The wordlength N is checked to see if it is valid with the present data.
         *
         * n              the produced wordlength.
         *
         * s              the number of bits determined in all full stages.
         *
```

```
* inc           the number of input values checked between two adjacent quantization levels.
*
* vr            the converters voltage reference.
*
* vco           the internal ADC's comparator offset voltage.
*
* vse           the voltage reference independent voltage offset terms.
*
* vd            the term used for correction if the internal ADC produces the lowest quantuzation level.
*
* kr            the voltage reference coeficient.
*
* ksp           is contains all factors of ks that are not dependent on
*               the full stages wordlength s.
*
* lam           the subtractor's coeficient.
*
* abuf          used for the proposed converter simulation to take into account the buffer amp. gain.
*
* a             indicates if an algorithmic converter (a=0) or
*               a serial-flash converter (a!=0) is to be simulated.
*
* kpoint        used to specify that ever k_th point is to be printed out.
*
* mperr (IGNORED) is the maximum permissible error in LSBs
*               before an increased s is used,
*               processing continues until s >= 3 (SMAX).
*
* loc           is used for location compensation. The value used indicates how
*               many buffer amplifiers are between the input of the precision
*               gain stage and the enterance point of the precision gain circuit's
*               calibration voltage. Valid inputs are:2,1,0.
*/

if( scanf("%d %d %d",&n,&s,&inc) != 3 ) /* wordlength, bits per full stage, increment in steps to use */
        perror(1);
if( scanf("%f %f %f %f",&vr,&vco,&vse,&vd) != 4 ) /* stage voltages */
        perror(1);
if( scanf("%f %f %f %f",&kr,&ksp,&lam,&abuf) != 4 ) /* stage gain coefficients */
/* note ksp is used to derive ks if location compensation is required, otherwise ks = ksp */
        perror(1);
if( scanf("%d",&a) != 1 ) /* stage type: a=0 algo; a=1 flash */
        perror(1);
if( scanf("%d",&kpoint) != 1 ) /* this pram. indicates that every kpoint is to be printed out */
        perror(1);
if( scanf("%f",&mperr) != 1 ) /* maximum permissible error */
        perror(1);
```

```
if( scanf("%d",&loc) != 1 ) /* indicates a location compensation is required for ks
when other than 0 */
        perror(1);

if( s < 1 || s >= n ) /* insure valid data was entered */
        perror(2);

if( loc == NO )
        ks = ksp; /* no location compensation is required when the precision gain circuit is
        calibrated at its input */

if( kpoint == 0 ) /* print out every point */
        kpoint =1;
if( inc > IMAX || inc < 1 )  /* insure that the inc value is not to large or small */
        inc,= IMAX;
if(argv[1][0] == '-' && ( argv[1][1] == 'd' || argv[1][1] == 'D' ))
        dflag = YES;
else
{
        if(argv[2][0] == '-' && ( argv[2][1] == 'd' || argv[2][1] == 'D' ))
                dflag = YES;
        else
                dflag = NO;  /* choose data only mode with a -d or -D to set dflag = YES */
}
 if(argv[1][0] == '-' && ( argv[1][1] == 'm' || argv[1][1] == 'M' ))
 /* maximum values only when yes */
        mflag = YES;
 else
 {
        if(argv[2][0] == '-' && ( argv[2][1] == 'm' || argv[2][1] == 'M' ))
                mflag = YES;
        else
                mflag = NO;  /* choose data only mode with a -d or -D to set dflag = YES */
 }

 if( loc != NO )
        ks = ksp/( (vse/vr)*power(2,s)+1.0 ); /* location compensation */
 sim(n,s,kpoint,inc); /* simulate all the required input values */
}

float
sim(n,s,kpoint,inc)
int n,s,kpoint,inc;
{
/* This routine SIM is used to simulate the entire converter.
 * All the possible quantization levels are checked as can intermediate
 * ones. Values for the first error maximum occurance are formed in: emax (worst conversion error in lsbs)
 * vmax (input voltage at emax). THese values are printed out every k_th point.
* The absolute value of emax is returned by this routine.
*/
        extern  int dflag,mflag;
        extern  float vr,vse,vd,vco,kr,ks,lam,ie,veq,vin;
        int r,qmax,i,stages;
        int power(),stage(),datap();
        float emax,vlsb,vint,ler,vmax,vexp,j;

        emax = 0;  /*  initialize the error max.  */
        qmax = power(2,n);  /*  the number of quantization levels */
        vlsb = vr/qmax;  /* lsb's voltage */
        r = n % s; /* determine the number of bits in the partial stage */
        if( r == 0 )
                r = s;
        stages = ( n-r )/s; /* the number of full stages required */

        for( j = 0; j <= qmax-1; j += 1.0/inc )  /* generate all quantization levels in lsbs  */
        {
                vin = j*vr/qmax;  /* input to be digitized  */
                vint = vin;  /*  remains unchanged through out the conversion  */
                veq = 0; /* initialize digital pattern's voltage */

                /* CONVERTER */
                vin += vlsb/2;  /* add the 1/2 lsb before processing  */
                stage(s,NO,1);  /* first full stage, require parameter init.    */
                for( i = 2; i <= stages; i++ )
                        stage(s,NO,i);
                /* save the partial stage's input durring the next step */
                stage(r,YES,stages+1);  /* partial stage, must reinitialize the stage */
                /* exit with vin=vexp, and veq=' bit pattern voltage ' */
                /* END CONVERTER */

                ler = (veq-vint)/vlsb;  /* lsbs error  */

                if( abs(emax) < abs(ler) )
                {
                        emax = ler; /* record the worst case value, and the voltage it occured at */
                        vmax = vint;
                }


                if( mflag == NO && (int) j % kpoint == 0 ) /* every kpoint */
                /* print out the calculated values */
                        printf("%9.5f  %7.3f\n",vint,ler);
        }
if( dflag == NO )
{
        printf(" The worst case error is %4.2f LSBs, which occured at",emax);
        printf(" %6.4f volts input\n",vmax);
        printf("  N= %3d  s= %3d\n",n,s);
 }
 else
        printf("* %4.2f   %6.4f       %3d   %3d\n",emax,vmax,n,s);
 return( abs(emax) ); /* must return an abs value so that the mperr is not exceeded */
}


stage(b,x,i)
int b,i,x;
{
/* This program 'STAGE' is used to calculate the
* results for one stage of the converter (either full or partial stage).
* Both the algorithmic and serial flash converter can be realized.
*
* b      indicates the number of bits determined in the stage
* i      indicates the stage being worked on
* x      indicates when the partial stage is being simulated
*
* a = 0 implies algorithmic
* a != 0 implies flash
*/
        extern float vin,veq,vr,vco,vse,kr,ks,lam,ie,abuf;
        extern  int a,loc;
        static int amp,refmax,s;
        static int init = 0;
        static float compf;
        int j;
        int power();
        float vsi,vcomp,comf;
        float fpow();

        if( init == 0 || x == YES ) /* initialize stage parameters once per bit set, or when in the partial stage */
        {
                if( x == YES )
                        init = 0; /* allow next input to be simulated with new parameters */
                else
                {
                        init = 1; /* next input is only partially processed, use the old values */
                        s = b; /* save the number of bits produced by a full stage */
                }
                amp = power(2,b);  /*  algo. stage's ideal gain, also used in flash cal. */
                refmax = amp-1;  /*  max. reference factor  */
                compf = kr*vr/amp;  /*  comparator factor used to form the ref. voltage */
                if( a != 0 )
                        amp = 1;  /*  flash stage's gain  */
        }
        comf = (a != 0) ? compf/power(2,s*(i-1)):compf; /* depends on the stage type and the previous stages resolution */
        for( j = refmax; j >= 1; j-- )  /* create all possible stage references work from the highest to the lowest  */
        {
                vcomp = comf*j+vco;  /*  actual comparision voltage, depends on stage type */
                if( vcomp < vin ) /* if satisfied, then must reduce the input by the first voltage reference it is larger than */
                {
                        vsi = (comf*j+ie)/abuf; /* calibration pt. at buf1's input */
                        switch(loc)
                        {
                        default:
                                printf("error in loc input\n");
                                exit();
                        case 0:
                                vsi *= abuf; /* cal. pt. at pre1's input */
                        case 1:
                                vsi *= abuf; /* cal. pt. at buf2's input */
                        case 2:
                                ; /* cal. pt. at buf1's input */
                        }
                        veq += j*vr/power(2,b+s*(i-1)); /*  ideal pattern voltage  */
                        j = 1;  /* terminate next block's condition  */
                }
                else
                        if( j == 1 ) /* no subtraction if vin < vcomp, last ref. voltage checked here */
                                vsi = vd/kr; /* make a vd adjustment if the lowest quantization level was produced */
        }
        if( x == NO )  /*  leaves vin at vexp when in the partial stage */
                vin = ( fpow(abuf,2-loc)*vin-lam*(kr*vsi+vse) )*ks*amp; /* location adjustment */
}
/*      ***     */

int
power(base,exp)
int base,exp;
{
/*  base is raised to the power of exp, both are positive int values */
        int value;
        for( value = 1; exp > 0; value *= base, exp-- )
        ;
        return(value);
}
/*      ***     */

float
fpow(base,exp)
int exp;
float base;
```

```
{
/*  base is raised to the power of exp, exp is a positive int value
 *  a floating point return is made
 */
        float value;
        for( value = 1.0; exp > 0; value *= base, exp-- )
        ;
        return(value);
}
/*      ***      */

int
perror(e)
int e;
{
switch(e)
{
default:
        printf("data error\n");
        exit();
case 1:
        printf("error in the data input\n");
        exit();
case 2:
        printf("parameter 's' is invalid\n");
        exit();
 }
}
```

```
/* THIS PROGRAM 'NMAX' IS USED TO SIMULATE A COMPLETE CONVERTER
 *  EITHER THE ALGORITHMIC OR SERIAL-FLASH CONVERTER IT FINDS THE VARIOUS
 *  COMBINATIONS OF WORDLENGTH AND s THAT DO NOT EXCEED THE MAXIMUM PERMISSIBLE
 *  ERROR (MPERR). THE VALUE s CAN HAVE A VALUE BETWEEN 1 AND 3 WITH OUT PROGRAM
 *  MODIFICATION (SMAX). TO PRODUCE DATA ONLY USE A -D OR -d SWITCH, THIS WILL
 *  FLAG MAXIMUM VALUES WITH A * IN THE FIRST COLUMN. TO PRODUCE ONLY THE MAXIMUM
 *  VALUES USE A -M OR A -m SWITCH. THE SWITCHES MAY ALSO BE COMBINED IF SEPARATED
 *  WITH AT LEAST ONE SPACE.
 */

#define YES 1
#define NO 0
#define SMAX 3
#define INCMAX 12
#define abs(x) (((x)>0)?(x):-(x))

float vin,veq,vr,vse,vd,vco,kr,ks,lam,ie,abuf,mperr;
int a,dflag,mflag,loc;

main(argc,argv)
int argc;
char *argv[];

{        extern  int a,dflag,mflag,loc;
         extern  float vr,vse,vd,vco,kr;
         extern  float ks,lam,ie,abuf,mperr;
         int n,s,inc,kpoint,first;
         int perror();
         float ksp;
         float sim();

         /* INPUT VALUES
          * n    s      inc
          * vr   vco    vse   vd
          * kr   ksp    lam   abuf
          * a
          * kpoint
          * mperr
          * loc
          *
          * A check for the correct number of data elements is made
          * and the inc size is checked to insure that no more than 12 steps (INCMAX) are used
          * and that it is not to small.
          * Parameter 's' is checked as to its validity.
          * The wordlength N is checked to see if it is valid with the present data.
          *                the produced wordlength.
          * n
          *
```

```
* s             the number of bits determined in all full stages.
*
* inc           the number of input values checked between two adjacent quantization levels.
*
* vr            the converters voltage reference.
*
* vco           the internal ADC's comparator offset voltage.
*
* vse           the voltage reference independent voltage offset terms.
*
* vd            the term used for correction if the internal ADC produces the lowest quantization level.
*
* kr            the voltage reference coeficient.
*
* ksp           is contains all factors of ks that are not dependent on
*               the full stages wordlength s.
*
* lam           the subtractor's coeficient.
*
* abuf          used for the proposed converter simulation to take into account the buffer amp. gain.
*
* a             indicates if an algorithmic converter (a=0) or
*               a serial-flash converter (a!=0) is to be simulated.
*
* kpoint        used to specify that ever k_th point is to be printed out.
*
* mperr         is the maximum permissible error in LSBs
*               before an increased s is used,
*               processing continues until s >= 3 (SMAX).
*
* loc           is used for location compensation. The value used indicates how
*               many buffer amplifiers are between the input of the precision
*               gain stage and the enterance point of the precision gain circuit's
*               calibration voltage. Valid inputs are:2,1,0.
*/

if( scanf("%d %d %d",&n,&s,&inc) != 3 ) /* wordlength, bits per full stage, increment in steps to use */
        perror(1);
if( scanf("%f %f %f %f",&vr,&vco,&vse,&vd) != 4 ) /* stage voltages */
        perror(1);
if( scanf("%f %f %f %f",&kr,&ksp,&lam,&abuf) != 4 ) /* stage gain coefficients */
/* note ksp is used to derive ks if location compensation is required, otherwise ks = ksp */
        perror(1);
if( scanf("%d",&a) != 1 ) /* stage type: a=0 algo; a=1 flash */
        perror(1);
if( scanf("%d",&kpoint) != 1 ) /* this pram. indicates that every kpoint is to be printed out */
        perror(1);
if( scanf("%f",&mperr) != 1 ) /* maximum permissible error */
```

```
        perror(1);
if( scanf("%d",&loc) != 1 ) /* indicates a location compensation is required for ks
when other than 0 */
        perror(1);

if( s < 1 || s >= n ) /* insure valid data was entered */
        perror(2);

if( loc == NO )
        ks = ksp; /* no location compensation is required when the precision gain circuit is
        calibrated at its input */

if( kpoint == 0 ) /* print out every point */
        kpoint =1;
if( inc > INCMAX || inc < 1 )  /* insure that the inc value is not to large or small */
        inc = INCMAX;
if(argv[1][0] == '-' && ( argv[1][1] == 'd' || argv[1][1] == 'D' ))
        dflag = YES;

else
{       if(argv[2][0] == '-' && ( argv[2][1] == 'd' || argv[2][1] == 'D' ))
                dflag = YES;

        else    dflag = NO;  /* choose data only mode with a -d or -D to set dflag = YES */

}
if(argv[1][0] == '-' && ( argv[1][1] == 'm' || argv[1][1] == 'M' ))
/* maximum values only when yes */
        mflag = YES;

else
{       if(argv[2][0] == '-' && ( argv[2][1] == 'm' || argv[2][1] == 'M' ))
                mflag = YES;

        else    mflag = NO;  /* choose data only mode with a -d or -D to set dflag = YES */

}

while( s <= SMAX )
{       if( loc != NO )
                ks = ksp/( (vse/vr)*power(2,s)+1.0 ); /* location compensation performed here */
        first = YES;  /* first start of simulation run */
        while( first == YES )
        {       while( sim(n,s,kpoint,inc) < mperr ) /* note the absolute value of the maximum error is returned */
                {       n++;
```

```
                                first = NO;  /* wordlength has increased, simulation has started */
                        }
                        n--;  /* if initial wordlength is too large, reduce, first is still YES */
                }
                if( dflag == NO )
                        printf("The maximum permissible error of %3.1f LSB's was exceeded after n=%2d with s=%2d\n",mperr,n,s);
                else
                        printf("* %3.1f   %2d   %2d\n",mperr,n,s);
                s++;
        }
}

float
sim(n,s,kpoint,inc)
int n,s,kpoint,inc;
{
/* This routine SIM is used to simulate the entire converter.
 * All the possible quantization levels are checked as can intermediate
 * ones. Values for the first error maximum occurance are formed in: emax (worst conversion error in lsbs)
 * vmax (input voltage at emax). These values are printed out every k_th point.
 * The absolute value of emax is returned by this routine.
 */
        extern  int dflag,mflag;
        extern  float vr,vse,vd,vco,kr,ks,lam,ie,veq,vin,mperr;
        int r,qmax,i,stages;
        int power(),stage(),datap();
        float emax,vlsb,vint,ler,vmax,vexp,j;

        emax = 0;  /*  initialize the error max.  */
        qmax = power(2,n);  /*  the number of quantization levels */
        vlsb = vr/qmax;  /* lsb's voltage */
        r = n % s; /* determine the number of bits in the partial stage */
        if( r == 0 )
                r = s;
        stages = ( n-r )/s; /* the number of full stages required */

        for( j = 0; j <= qmax-1; j += 1.0/inc )  /* generate all quantization levels in lsbs  */
        {
                vin = j*vr/qmax;  /* input to be digitized  */
                vint = vin;  /*  remains unchanged through out the conversion  */
                veq = 0; /* initialize digital pattern's voltage */

                /* CONVERTER */
                vin += vlsb/2;  /* add the 1/2 lsb before processing  */
                stage(s,NO,1);  /* first full stage, require parameter init.    */
                for( i = 2; i <= stages; i++ )
                        stage(s,NO,1);
                /* save the partial stage's input durring the next step */
                stage(r,YES,stages+1);  /* partial stage, must reinitialize the stage */
                /* exit with vin=vexp, and veq=' bit pattern voltage ' */
                /* END CONVERTER */

                ler = (veq-vint)/vlsb;  /* lsbs error  */

                if( abs(emax) < abs(ler) )
                {
                        emax = ler; /* record the worst case value, and the voltage it occured at */
                        vmax = vint;
                        if( abs(emax) > abs(mperr) )
                                j = qmax; /* terminate the conversion once mperr has been exceeded */
                }


                if( mflag == NO && (int) j % kpoint == 0 ) /* every kpoint */
                /* print out the calculated values */
                        printf("%9.5f  %7.3f\n",vint,ler);
        }
 if( dflag == NO )
 {
        printf(" The worst case error is %4.2f LSBs, which occured at",emax);
        printf(" %6.4f volts input\n",vmax);
        printf("  N= %3d  s= %3d\n",n,s);
 }
 else
        printf("* %4.2f   %6.4f      %3d   %3d\n",emax,vmax,n,s);
 return( abs(emax) ); /* must return an abs value so that the mperr is not exceeded */
}


stage(b,x,i)
int b,i,x;
{
/* This program 'STAGE' is used to calculate the
* results for one stage of the converter (either full or partial stage).
* Both the algorithmic and serial flash converter can be realized.
*
* b     indicates the number of bits determined in the stage
* i     indicates the stage being worked on
* x     indicates when the partial stage is being simulated
*
* a = 0 implies algorithmic
* a != 0 implies flash
*/
        extern float vin,veq,vr,vco,vse,kr,ks,lam,ie,abuf;
        extern  int a,loc;
        static int amp,refmax,s;
static int init = 0;
static float compf;
int j;
int power();
float vsi,vcomp,comf;
float fpow();

if( init == 0 || x == YES ) /* initialize stage parameters once per bit set, or when in the partial stage */
{
        if( x == YES )
                init = 0; /* allow next input to be simulated with new parameters */
        else
        {
                init = 1; /* next input is only partially processed, use the old values */
                s = b; /* save the number of bits produced by a full stage */
        }
        amp = power(2,b);  /*  algo. stage's ideal gain, also used in flash cal. */
        refmax = amp-1;  /*  max. reference factor  */
        compf = kr*vr/amp;  /*  comparator factor used to form the ref. voltage */
        if( a != 0 )
                amp = 1;  /*  flash stage's gain  */
}
comf = (a != 0) ? compf/power(2,s*(i-1)):compf; /* depends on the stage type and the previous stages resolution */
for( j = refmax; j >= 1; j-- )  /* create all possible stage references work from the highest to the lowest  */
{
        vcomp = comf*j+vco;  /*  actual comparision voltage, depends on stage type */
        if( vcomp < vin ) /* if satisfied, then must reduce the input by the first voltage reference it is larger than */
        {
                vsi = (comf*j+ie)/abuf; /* calibration pt. at bufi's input */
                switch(loc)
                {
                default:
                        printf("error in loc input\n");
                        exit();
                case 0:
                        vsi *= abuf; /* cal. pt. at prei's input */
                case 1:
                        vsi *= abuf; /* cal. pt. at buf2's input */
                case 2:
                        ; /* cal. pt. at bufi's input */
                }
                veq += j*vr/power(2,b+s*(i-1)); /*  ideal pattern voltage  */
                j = 1;  /* terminate next block's condition  */
        }
        else
                if( j == 1 ) /* no subtraction if vin < vcomp, last ref. voltage checked here */
                        vsi = vd/kr; /* make a vd adjustment if the lowest quantization level was produced */
}
```

```
        if( x == NO )  /*  leaves vin at vexp when in the partial stage */
                vin = ( fpow(abuf,2-loc)*vin-lam*(kr*vsi+vse) )*ks*amp; /* location adjustment */
}
/*      ***     */

int
power(base,exp)
int base,exp;
{
/*  base is raised to the power of exp, both are positive int values */
        int value;
        for( value = 1; exp > 0; value *= base, exp-- )
        ;
        return(value);
}
/*      ***     */

float
fpow(base,exp)
int exp;
float base;
{
/*  base is raised to the power of exp, exp is a positive int value
 *  a floating point return is made
 */
        float value;
        for( value = 1.0; exp > 0; value *= base, exp-- )
        ;
        return(value);
}
/*      ***     */

int
perror(e)
int e;
{
switch(e)
{
default:
        printf("data error\n");
        exit();
case 1:
        printf("error in the data input\n");
        exit();
case 2:
        printf("parameter 's' is invalid\n");
        exit();
}
}
```

APPENDIX TWO

This appendix includes several SPICE simulations of the designed buffer amplifier previously discussed in chapter 3.

```
*******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER

****     INPUT LISTING                     TEMPERATURE =   27.000 DEG C

********************************************************************


*
.DC VIN 0 3 .25
.PLOT DC  V(13,1) V(3,5) V(6,12)
.PRINT DC V(13,1) V(3,5) V(6,12) V(6,9)
.AC DEC 10 1K 1000MEG
.PLOT AC VDB(13) VDB(6)
VIN 1 0 DC 1 AC 1 PULSE(1 0 0 0 0 350N 1)
.TRAN 10N 750N
.PLOT TRAN V(13) V(6) V(12)
*
* LOAD
CL 13 0 1P
*
*  INPUT STAGE
M1 3 1 2 14 MN 10U 100U
M2 5 5 2 14 MN 10U 100U
M3 6 6 5 15 MN 10U 100U
M6 6 8 7 7 MP 20U 225U
M7 7 6 3 15 MN 10U 100U
M13 2 10 11 11 MN 25U 80U
*
*   BUFFER OUTPUT STAGE
M4 12 6 13 15 MN 10U 100U
M5 13 12 7 7 MP 10U 200U
M11 12 8 7 7 MP 20U 225U
M12 13 10 11 11 MN 20U 80U
*
*  BIAS CICUIT
M8 10 10 11 11 MN 25U 40U
M9 10 5 9 7 MP 10U 300U
M10 9 8 7 7 MP 20U 225U
M14 8 8 7 7 MP 10U 118U
I1 8 0 20U
*
* SUBSTRATE BIAS
VSUB1 14 0 -2.0
```

```
VSUB2 15 0 -0.001
*
VDD 7 0 5
VSS 0 11 5
*
.WIDTH IN=80 OUT=80
.OPT NOMOD
*
.MODEL MP PMOS (LEVEL=2 VTO=-.9 KP=9.75E-6 GAMMA=.634
+PHI=.612  RD=2.0 RS=2.00 CBD=2.0E-14
+CBS=2.0E-14 IS=1.0E-14 PB=.7 CGSO=2.44E-10
+CGDO=2.44E-10 CGBO=2.0E-12 RSH=75.0
+CJ=1.54E-4 MJ=.5 CJSW=4.37E-10 MJSW=.5
+JS=4.19E-10 TOX=8.5E-8 NSUB=1.98E15 TPG=1.0
+XJ=9.0E-7 LD=6.0E-7 U0=240 UCRIT=6.44E4
+UEXP=0.139 VMAX=7.33E4 XQC=0.4)
*
.MODEL MN NMOS (LEVEL=2 VTO=.9 KP=3.05E-5 GAMMA=1.592
+PHI=.695  RD=2.0 RS=2.00 CBD=2.0E-14
+CBS=2.0E-14 IS=1.0E-14 PB=.7 CGSO=2.84E-10
+CGDO=2.84E-10 CGBO=2.0E-12 RSH=15.0
+CJ=3.44E-4 MJ=.5 CJSW=1.09E-9 MJSW=.5
+JS=1.37E-5 TOX=8.5E-8 NSUB=9.92E15 TPG=1.0
+XJ=1.0E-6 LD=7.0E-7 U0=750 UCRIT=1.23E5
+UEXP=0.022 VMAX=4.92E5 XQC=0.4)
*
.END
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER


****     DC TRANSFER CURVES                    TEMPERATURE =   27.000 DEG C


******************************************************************************



  VIN           V(13,1)      V(3,5)       V(6,12)      V(6,9)


0.000e+00      1.353e-02    1.423e-02   -2.333e+00   -5.294e-01
2.500e-01      1.030e-02    1.304e-02   -1.895e+00   -3.108e-01
5.000e-01      6.616e-03    1.131e-02   -1.480e+00   -1.141e-01
7.500e-01      2.564e-03    9.169e-03   -1.081e+00    6.720e-02
1.000e+00     -1.808e-03    6.702e-03   -6.940e-01    2.370e-01
1.250e+00     -6.476e-03    3.951e-03   -3.173e-01    3.980e-01
```

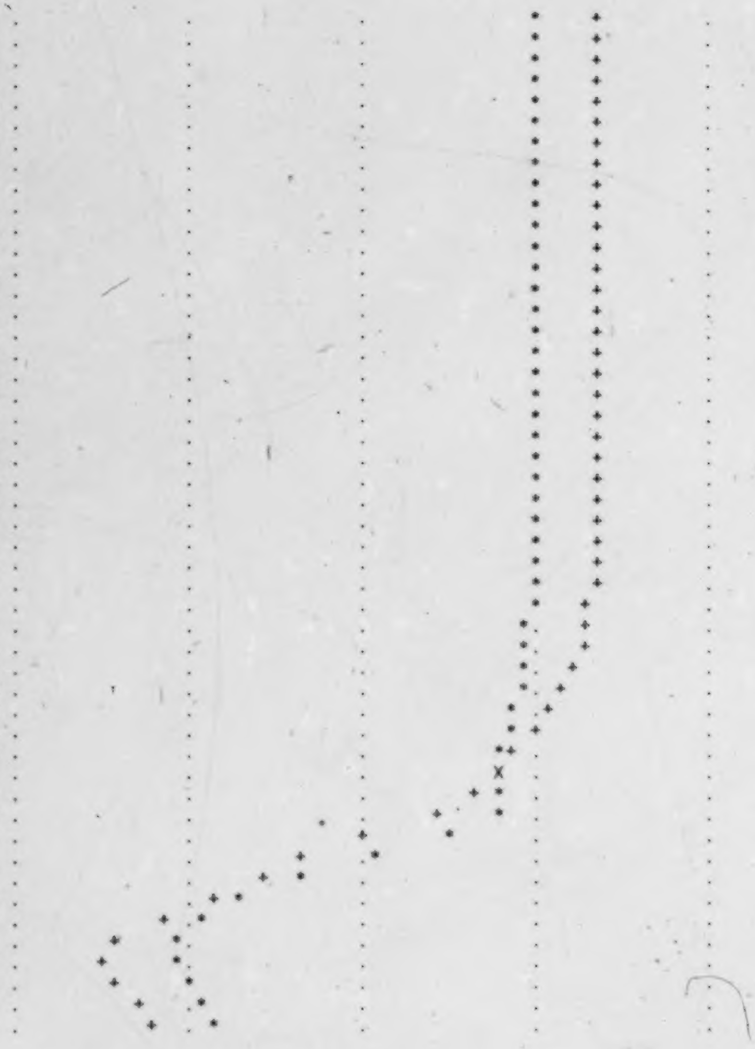
```
1.500e+00    -1.146e-02    9.403e-04    5.093e-02    5.518e-01
1.750e+00    -1.679e-02   -2.345e-03    4.120e-01    6.999e-01
2.000e+00    -2.254e-02   -5.914e-03    7.670e-01    8.435e-01
2.250e+00    -5.724e-02   -2.422e-02    1.076e+00    9.606e-01
2.500e+00    -1.993e-01   -9.581e-02    1.229e+00    9.890e-01
2.750e+00    -3.782e-01   -1.828e-01    1.329e+00    9.831e-01
3.000e+00    -5.826e-01   -2.775e-01    1.393e+00    9.501e-01

*******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER

****     DC TRANSFER CURVES                 TEMPERATURE =   27.000 DEG C

**********************************************************************


LEGEND:

*: V(13,1)
+: V(3,5)
=: V(6,12)

  VIN        V(13,1)

*)------------- -6.000d-01    -4.000d-01    -2.000d-01     0.000d+00  2.000d-01
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

+)------------- -3.000d-01    -2.000d-01    -1.000d-01     0.000d+00  1.000d-01
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

=)------------- -4.000d+00    -2.000d+00     0.000d+00     2.000d+00  4.000d+00
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
0.000d+00  1.353d-02 .           = .             .             .*+           .
2.500d-01  1.030d-02 .             .=            .             .*+           .
5.000d-01  6.616d-03 .             .   =         .             * +           .
7.500d-01  2.564d-03 .             .     =       .             *+            .
1.000d+00 -1.808d-03 .             .        =    .             *+            .
1.250d+00 -6.476d-03 .             .           = .             *+            .
1.500d+00 -1.146d-02 .             .             =            *+             .
1.750d+00 -1.679d-02 .             .             .  =         *+             .
2.000d+00 -2.254d-02 .             .             .    =      *+.             .
2.250d+00 -5.724d-02 .             .             .       = *+  .             .
2.500d+00 -1.993d-01 .             .             *+       =    .             .
2.750d+00 -3.782d-01 .             . X           .        =    .             .
```

```
3.000d+00 -5.826d-01 .* +                      =
                     - - - - - - - - - - - - - - - - - - - - - - - - - - -


 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    1.0000    (  2)   -0.9461    (  3)    0.9990    (  5)    0.9923
(  6)    2.8985    (  7)    5.0000    (  8)    3.5078    (  9)    2.6615
( 10)   -3.0407    ( 11)   -5.0000    ( 12)    3.5925    ( 13)    0.9982
( 14)   -2.0000    ( 15)   -0.0010


    VOLTAGE SOURCE CURRENTS

    NAME        CURRENT

    VIN        0.000d+00

    VSUB1      1.123d-11

    VSUB2      2.009d-11

    VDD       -1.143d-04

    VSS       -9.432d-05

    TOTAL POWER DISSIPATION   9.73d-04  WATTS
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****
```

```
BUFFER AMPLIFIER

****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

**************************************************************************


**** MOSFETS


               M1          M2          M3          M6          M7          M13         M4

MODEL        MN          MN          MN          MP          MN          MN          MN
ID             1.72e-05    1.65e-05    1.65e-05   -1.65e-05    1.72e-05    3.36e-05    1.63e-05
VGS              1.946       1.938       1.906      -1.492       1.900       1.959       1.900
VDS              1.945       1.938       1.906      -2.101       4.001       4.054       2.594
VBS             -1.054      -1.054      -0.993       0.         -1.000       0.         -0.999
VTH              1.563       1.563       1.529      -0.882       1.520       0.876       1.528
VDSAT            0.247       0.242       0.241      -0.457       0.244       0.605       0.239
GM             8.97e-05    8.79e-05    8.76e-05    5.44e-05    9.07e-05    6.35e-05    8.75e-05
GDS            9.00e-07    8.78e-07    8.76e-07    3.07e-07    6.84e-07    2.29e-07    7.83e-07
GMB            4.76e-05    4.66e-05    4.73e-05    1.79e-05    4.87e-05    4.98e-05    4.71e-05
CBD            8.70e-15    8.71e-15    8.82e-15    1.00e-14    7.01e-15    7.67e-15    8.08e-15
CBS            1.26e-14    1.26e-14    1.29e-14    2.00e-14    1.28e-14    2.00e-14    1.28e-14
CGSOVL         2.84e-14    2.84e-14    2.84e-14    5.49e-14    2.84e-14    2.27e-14    2.84e-14
CGDOVL         2.84e-14    2.84e-14    2.84e-14    5.49e-14    2.84e-14    2.27e-14    2.84e-14
CGBOVL         1.72e-17    1.72e-17    1.72e-17    3.76e-17    1.72e-17    4.72e-17    1.72e-17
DERIVATIVES OF GATE (DQGDVX) AND BULK (DQBDVX) CHARGES
DQGDVGB        2.74e-13    2.74e-13    2.75e-13    1.28e-12    2.75e-13    6.18e-13    2.75e-13
DQGDVDB        0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
DQGDVSB       -2.33e-13   -2.33e-13   -2.33e-13   -1.15e-12   -2.33e-13   -5.18e-13   -2.33e-13
DQBDVGB       -4.13e-14   -4.13e-14   -4.18e-14   -1.47e-13   -4.15e-14   -1.18e-13   -4.17e-14
DQBDVDB        0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
DQBDVSB       -1.31e-13   -1.31e-13   -1.33e-13   -4.15e-13   -1.32e-13   -4.43e-13   -1.32e-13


               M5          M11         M12         M8          M9          M10         M14

MODEL        MP          MP          MN          MN          MP          MP          MP
ID            -2.79e-05   -1.62e-05    4.42e-05    1.65e-05   -1.65e-05   -1.65e-05   -2.00e-05
```

```
VGS         -1.408     -1.492      1.959      1.959     -1.669     -1.492     -1.492
VDS         -4.002     -1.408      5.998      1.959     -5.702     -2.338     -1.492
VBS          0.         0.         0.         0.         2.338      0.         0.
VTH         -0.856     -0.883      0.866      0.879     -1.352     -0.881     -0.863
VDSAT       -0.414     -0.456      0.613      0.602     -0.272     -0.457     -0.472
GM        1.02e-04   5.38e-05   8.26e-05   3.13e-05   1.04e-04   5.46e-05   6.39e-05
GDS       9.07e-07   3.51e-07   3.15e-07   1.56e-07   6.91e-07   2.96e-07   9.05e-07
GMB       3.13e-05   1.77e-05   6.40e-05   2.46e-05   1.52e-05   1.80e-05   1.96e-05
CBD       7.72e-15   1.15e-14   6.47e-15   1.03e-14   5.66e-15   9.60e-15   1.13e-14
CBS       2.00e-14   2.00e-14   2.00e-14   2.00e-14   9.60e-15   2.00e-14   2.00e-14
CGSOVL    4.88e-14   5.49e-14   2.27e-14   1.14e-14   7.32e-14   5.49e-14   2.88e-14
CGDOVL    4.88e-14   5.49e-14   2.27e-14   1.14e-14   7.32e-14   5.49e-14   2.88e-14
CGBOVL    1.76e-17   3.76e-17   3.72e-17   4.72e-17   1.76e-17   3.76e-17   1.76e-17
DERIVATIVES OF GATE (DQGDVX) AND BULK (DQBDVX) CHARGES
DQGDVGB   5.37e-13   1.28e-12   4.86e-13   3.09e-13   7.69e-13   1.28e-12   3.17e-13
DQGDVDB   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00
DQGDVSB  -4.79e-13  -1.15e-12  -4.08e-13  -2.59e-13  -7.15e-13  -1.15e-12  -2.83e-13
DQBDVGB  -5.72e-14  -1.47e-13  -9.22e-14  -5.89e-14  -4.77e-14  -1.47e-13  -3.37e-14
DQBDVDB   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00
DQBDVSB  -1.64e-13  -4.16e-13  -3.46e-13  -2.22e-13  -1.14e-13  -4.15e-13  -9.77e-14
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER

****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C

*******************************************************************************


LEGEND:

*: VDB(13)
+: VDB(6)

    FREQ      VDB(13)

*)------------- -6.000d+01    -4.000d+01    -2.000d+01     0.000d+00  2.000d+01
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

+)------------- -3.000d+01    -2.000d+01    -1.000d+01     0.000d+00  1.000d+01
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
1.000d+03 -1.587d-01 .             .             .             *    +        .
1.259d+03 -1.587d-01 .             .             .             *    +        .
1.585d+03 -1.587d-01 .             .             .             *    +        .
1.995d+03 -1.587d-01 .             .             .             *    +        .
```

```
2.512d+03 -1.587d-01
3.162d+03 -1.587d-01
3.981d+03 -1.587d-01
5.012d+03 -1.587d-01
6.310d+03 -1.587d-01
7.943d+03 -1.587d-01
1.000d+04 -1.587d-01
1.259d+04 -1.587d-01
1.585d+04 -1.587d-01
1.995d+04 -1.588d-01
2.512d+04 -1.588d-01
3.162d+04 -1.588d-01
3.981d+04 -1.589d-01
5.012d+04 -1.590d-01
6.310d+04 -1.592d-01
7.943d+04 -1.594d-01
1.000d+05 -1.599d-01
1.259d+05 -1.605d-01
1.585d+05 -1.616d-01
1.995d+05 -1.633d-01
2.512d+05 -1.660d-01
3.162d+05 -1.703d-01
3.981d+05 -1.774d-01
5.012d+05 -1.888d-01
6.310d+05 -2.075d-01
7.943d+05 -2.386d-01
1.000d+06 -2.907d-01
1.259d+06 -3.773d-01
1.585d+06 -5.184d-01
1.995d+06 -7.371d-01
2.512d+06 -1.052d+00
3.162d+06 -1.469d+00
3.981d+06 -1.978d+00
5.012d+06 -2.559d+00
6.310d+06 -3.173d+00
7.943d+06 -3.742d+00
1.000d+07 -4.099d+00
1.259d+07 -4.009d+00
1.585d+07 -4.283d+00
1.995d+07 -1.004d+01
2.512d+07 -1.897d+01
3.162d+07 -2.735d+01
3.981d+07 -3.426d+01
5.012d+07 -3.879d+01
6.310d+07 -4.100d+01
7.943d+07 -4.107d+01
1.000d+08 -3.992d+01
1.259d+08 -3.865d+01
1.585d+08 -3.766d+01
```

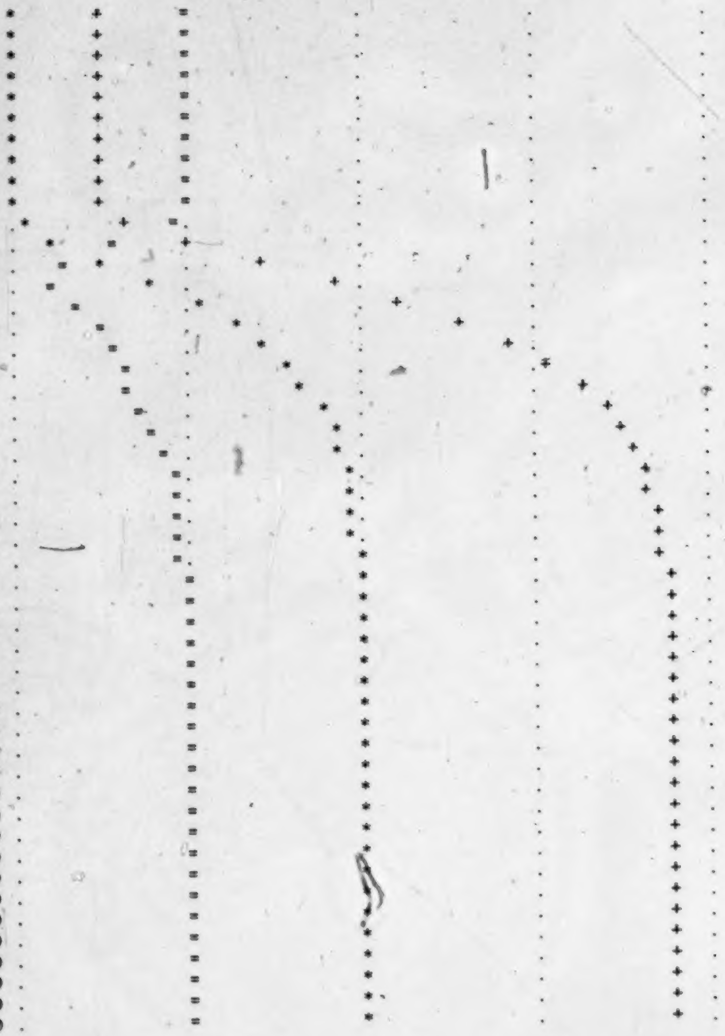


```
1.995d+08 -3.698d+01 .           + . *            .             .             .
2.512d+08 -3.652d+01 .            +. *            .             .             .
3.162d+08 -3.622d+01 .            +   *           .             .             .
3.981d+08 -3.602d+01 .            +   *           .             .             .
5.012d+08 -3.590d+01 .             +  *           .             .             .
6.310d+08 -3.582d+01 .             +  *           .             .             .
7.943d+08 -3.577d+01 .             +  *           .             .             .
1.000d+09 -3.574d+01 .             +  *           .             .             .
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -


*******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER

****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

*******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(   1)    1.0000   (   2)   -0.9461   (   3)    0.9990   (   5)    0.9923

(   6)    2.8985   (   7)    5.0000   (   8)    3.5078   (   9)    2.6615

(  10)   -3.0407   (  11)   -5.0000   (  12)    3.5925   (  13)    0.9982

(  14)   -2.0000   (  15)   -0.0010


    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VIN        0.000d+00

    VSUB1      1.123d-11

    VSUB2      2.009d-11
```

```
     VDD      -1.143d-04

     VSS      -9.432d-05

     TOTAL POWER DISSIPATION   9.73d-04  WATTS
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER

****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

**********************************************************************



**** MOSFETS


             M1          M2          M3          M6          M7          M13         M4

MODEL       MN          MN          MN          MP          MN          MN          MN
ID          1.72e-05    1.65e-05    1.65e-05   -1.65e-05    1.72e-05    3.36e-05    1.63e-05
VGS            1.946       1.938       1.906      -1.492       1.900       1.959       1.900
VDS            1.945       1.938       1.906      -2.101       4.001       4.054       2.594
VBS           -1.054      -1.054      -0.993       0.         -1.000       0.         -0.999


             M5          M11         M12         M8          M9          M10         M14

MODEL       MP          MP          MN          MN          MP          MP          MP
ID         -2.79e-05   -1.62e-05    4.42e-05    1.65e-05   -1.65e-05   -1.65e-05   -2.00e-05
VGS           -1.408      -1.492       1.959       1.959      -1.669      -1.492      -1.492
VDS           -4.002      -1.408       5.998       1.959      -5.702      -2.338      -1.492
VBS            0.          0.          0.          0.          2.338       0.          0.
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:26:49*****

BUFFER AMPLIFIER

****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C
```

```
***********************************************************************


LEGEND:

*: V(13)
+: V(6)
=: V(12)

    TIME      V(13)

*)-------------  0.000d+00     5.000d-01     1.000d+00     1.500d+00  2.000d+00
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

+)-------------  1.000d+00     1.500d+00     2.000d+00     2.500d+00  3.000d+00
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

=)-------------  3.400d+00     3.600d+00     3.800d+00     4.000d+00  4.200d+00
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
0.000d+00  9.982d-01 .            =.             *             .          +  .
1.000d-08  9.720d-01 .             =            *.             .       +     .
2.000d-08  8.836d-01 .             .     =    *  .             .  +          .
3.000d-08  7.412d-01 .             .      *   =  .           + .             .
4.000d-08  5.888d-01 .             . *           .=    +       .             .
5.000d-08  4.534d-01 .            *.             =+            .             .
6.000d-08  3.448d-01 .         *   .          X  .             .             .
7.000d-08  2.587d-01 .      *      .      X      .             .             .
8.000d-08  2.099d-01 .     *       .   +=        .             .             .
9.000d-08  1.719d-01 .    *        . +=          .             .             .
1.000d-07  1.419d-01 .   *         + =           .             .             .
1.100d-07  1.157d-01 .  *         +. =           .             .             .
1.200d-07  9.258d-02 .  *        + . =           .             .             .
1.300d-07  7.247d-02 . *        +  .=            .             .             .
1.400d-07  5.999d-02 . *       +   =             .             .             .
1.500d-07  5.085d-02 .*        +   =             .             .             .
1.600d-07  4.417d-02 .*       +    =             .             .             .
1.700d-07  3.838d-02 .*       +    =             .             .             .
1.800d-07  3.246d-02 .*      +     =             .             .             .
1.900d-07  2.656d-02 .*      +     =             .             .             .
2.000d-07  2.193d-02 .*      +     =             .             .             .
2.100d-07  1.884d-02 .*      +     =             .             .             .
2.200d-07  1.696d-02 *       +    =.             .             .             .
2.300d-07  1.618d-02 *       +    =.             .             .             .
2.400d-07  1.516d-02 *       +    =.             .             .             .
2.500d-07  1.395d-02 *      +      =             .             .             .
2.600d-07  1.264d-02 *      +      =             .             .             .
```

```
2.700d-07   1.170d-02
2.800d-07   1.109d-02
2.900d-07   1.110d-02
3.000d-07   1.110d-02
3.100d-07   1.106d-02
3.200d-07   1.072d-02
3.300d-07   1.053d-02
3.400d-07   1.050d-02
3.500d-07   1.096d-02
3.600d-07   1.145d-02
3.700d-07   2.463d-02
3.800d-07   1.028d-01
3.900d-07   2.477d-01
4.000d-07   3.986d-01
4.100d-07   5.269d-01
4.200d-07   6.301d-01
4.300d-07   7.045d-01
4.400d-07   7.725d-01
4.500d-07   8.346d-01
4.600d-07   8.845d-01
4.700d-07   9.189d-01
4.800d-07   9.422d-01
4.900d-07   9.513d-01
5.000d-07   9.593d-01
5.100d-07   9.670d-01
5.200d-07   9.768d-01
5.300d-07   9.853d-01
5.400d-07   9.921d-01
5.500d-07   9.944d-01
5.600d-07   9.952d-01
5.700d-07   9.953d-01
5.800d-07   9.964d-01
5.900d-07   9.982d-01
6.000d-07   1.000d+00
6.100d-07   1.001d+00
6.200d-07   1.002d+00
6.300d-07   1.001d+00
6.400d-07   1.001d+00
6.500d-07   1.001d+00
6.600d-07   1.001d+00
6.700d-07   1.001d+00
6.800d-07   1.001d+00
6.900d-07   1.001d+00
7.000d-07   1.000d+00
7.100d-07   1.000d+00
7.200d-07   1.000d+00
7.300d-07   1.000d+00
7.400d-07   1.000d+00
7.500d-07   1.000d+00
```



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- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

        JOB CONCLUDED

          TOTAL JOB TIME           113.90
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****

BUFFER AMPLIFIER

****     INPUT LISTING                     TEMPERATURE =   27.000 DEG C

*******************************************************************************

*
.DC VIN 0 3 .25
.PLOT DC I(VBOG) V(13,1) V(3,5) V(6,12)
.PRINT DC V(13,1) V(3,5) V(6,12) V(6,9)
.AC DEC 10 1K 1000MEG
.PLOT AC VDB(13) VDB(6)
VIN 1 0 DC 1 AC 1 PULSE(1 0 0 0 0 300N 1)
.TRAN 10N 750N
.PLOT TRAN V(13) V(6) V(12)
*
* LOAD
CL 13 0 1P
*
X1 1 13 30 7 11  TRANS
VBOG 30 6 0

*  INPUT STAGE
M1 3 1 2 14 MN 10U 100U
M2 5 5 2 14 MN 10U 100U
M3 6 6 5 15 MN 10U 100U
M6 6 8 7 7 MP 20U 50U
IMIN 6 0 4U
* THIS WAS INSERTED SO THAT SPICE WOULD CONVERGE
M7 7 6 3 15 MN 10U 100U
M13 2 10 11 11 MN 25U 80U
*
*   BUFFER OUTPUT STAGE
```

```
M4  12  6  13  15  MN  10U  100U
M5  13  12  7  7  MP  10U  200U
M11  12  8  7  7  MP  20U  225U
M12  13  10  11  11  MN  20U  80U
*
*  BIAS CICUIT
M8  10  10  11  11  MN  25U  40U
M9  10  5  9  7  MP  10U  300U
M10  9  8  7  7  MP  20U  225U
M14  8  8  7  7  MP  10U  118U
I1  8  0  20U
*
* SUBSTRATE BIAS
VSUB1  14  0  -2
VSUB2  15  0  0
*
VDD  7  0  5
VSS  0  11  5
*
.WIDTH IN=80 OUT=80
.OPT NOMOD
*
*TRANSCONDUCTANCE AMP
* NON INV OUT VDD VSS
.SUBCKT TRANS  4  1  6  9  8

M1  3  1  2  2  MN  20U  200U
M2  5  4  2  2  MN  20U  200U
M3  2  7  8  8  MN  20U  20U
M4  5  5  9  9  MP  20U  20U
M5  3  3  9  9  MP  20U  20U
M6  6  5  9  9  MP  30U  300U
M7  7  7  8  8  MN  20U  20U
*
IBIAS  0  7  4U
*
*     COMPENSATION
*CC  10  6  .5P
*RC  5  10  10K
.ENDS TRANS
*
.MODEL MP PMOS (LEVEL=2 VTO=-.9 KP=9.75E-6 GAMMA=.634
+PHI=.612  RD=2.0 RS=2.00 CBD=2.0E-14
+CBS=2.0E-14 IS=1.0E-14 PB=.7 CGSO=2.44E-10
+CGDO=2.44E-10 CGBO=2.0E-12 RSH=75.0
+CJ=1.54E-4 MJ=.5 CJSW=4.37E-10 MJSW=.5
+JS=4.19E-10 TOX=8.5E-8 NSUB=1.98E15 TPG=1.0
+XJ=9.0E-7 LD=6.0E-7 UO=240 UCRIT=6.44E4
+UEXP=0.139 VMAX=7.33E4 XQC=0.4)
```

```
*
.MODEL MN NMOS (LEVEL=2 VTO=.9 KP=3.05E-5 GAMMA=1.592
+PHI=.695  RD=2.0 RS=2.00 CBD=2.0E-14
+CBS=2.0E-14 IS=1.0E-14 PB=.7 CGSO=2.84E-10
+CGDO=2.84E-10 CGBO=2.0E-12 RSH=15.0
+CJ=3.44E-4 MJ=.5 CJSW=1.09E-9 MJSW=.5
+JS=1.37E-5 TOX=8.5E-8 NSUB=9.92E15 TPG=1.0
+XJ=1.0E-6 LD=7.0E-7 U0=750 UCRIT=1.23E5
+UEXP=0.022 VMAX=4.92E5 XQC=0.4)
*
.END
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****


BUFFER AMPLIFIER
                                        TEMPERATURE =   27.000 DEG C

****     DC TRANSFER CURVES

******************************************************************************


     VIN          V(13,1)       V(3,5)        V(6,12)       V(6,9)


  0.000e+00      2.101e-02     1.752e-02    -2.320e+00    -5.217e-01
  2.500e-01      2.074e-02     1.778e-02    -1.878e+00    -3.007e-01
  5.000e-01      2.036e-02     1.771e-02    -1.458e+00    -1.014e-01
  7.500e-01      1.988e-02     1.740e-02    -1.053e+00     8.259e-02
  1.000e+00      1.933e-02     1.691e-02    -6.617e-01     2.552e-01
  1.250e+00      1.869e-02     1.629e-02    -2.796e-01     4.191e-01
  1.500e+00      1.798e-02     1.556e-02     9.429e-02     5.759e-01
  1.750e+00      1.717e-02     1.472e-02     4.613e-01     7.272e-01
  2.000e+00      1.626e-02     1.379e-02     8.225e-01     8.741e-01
  2.250e+00     -2.247e-02    -6.583e-03     1.125e+00     9.878e-01
  2.500e+00     -1.710e-01    -8.200e-02     1.269e+00     1.012e+00
  2.750e+00     -3.774e-01    -1.824e-01     1.330e+00     9.834e-01
  3.000e+00     -5.995e-01    -2.848e-01     1.368e+00     9.348e-01
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****


BUFFER AMPLIFIER
                                        TEMPERATURE =   27.000 DEG C

****     DC TRANSFER CURVES
```

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*****************************************************************************


LEGEND:

*: I(VBOG)
+: V(13,1)
=: V(3,5)
$: V(6,12)

  VIN          I(VBOG)

*)-------------   0.000d+00       5.000d-06      1.000d-05      1.500d-05   2.000d-05
                        - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

+)-------------  -6.000d-01      -4.000d-01     -2.000d-01      0.000d+00   2.000d-01
                        - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

=)-------------  -3.000d-01      -2.000d-01     -1.000d-01      0.000d+00   1.000d-01
                        - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

$)-------------  -4.000d+00      -2.000d+00      0.000d+00      2.000d+00   4.000d+00
                        - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
0.000d+00   1.741d-05   .            $ .              .              .+=     *      .
2.500d-01   1.742d-05   .              .$             .              .+=     *      .
5.000d-01   1.745d-05   .              .   $          .              .+=     *      .
7.500d-01   1.748d-05   .              .      $       .              .+=     *      .
1.000d+00   1.752d-05   .              .         $    .              .+=     *      .
1.250d+00   1.757d-05   .              .            $ .              .+=     *      .
1.500d+00   1.762d-05   .              .              .$             .+=     *      .
1.750d+00   1.767d-05   .              .              .  $           .+=     *      .
2.000d+00   1.772d-05   .              .              .     $        .+=      *     .
2.250d+00   1.694d-05   .              .              .        $  .+=.    *         .
2.500d+00   1.330d-05                  .              . +=      X    .              .
2.750d+00   8.236d-06   .              . X       *    .         $    .              .
3.000d+00   4.519d-06   + =           *.              .          $   .              .
                        - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -


  *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****

BUFFER AMPLIFIER

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
```

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**********************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    1.0000    (  2)   -0.9407    (  3)    1.0253    (  5)    1.0084
(  6)    2.9307    (  7)    5.0000    (  8)    3.5078    (  9)    2.6755
( 10)   -3.0408    ( 11)   -5.0000    ( 12)    3.5923    ( 13)    1.0193
( 14)   -2.0000    ( 15)    0.        ( 30)    2.9307    ( 31)    3.3445
( 32)   -0.0148    ( 33)    3.4336    ( 34)   -3.4530


    VOLTAGE SOURCE CURRENTS

    NAME        CURRENT


    VIN       0.000d+00

    VBOG      1.752d-05

    VSUB1     1.130d-11

    VSUB2     2.021d-11

    VDD      -1.225d-04

    VSS      -1.025d-04

    TOTAL POWER DISSIPATION   1.03d-03  WATTS
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****

BUFFER AMPLIFIER

****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
```

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**********************************************************************

**** MOSFETS


            M1          M2          M3.         M6          M7          M13         M4

MODEL       MN          MN          MN          MP          MN          MN          MN
ID            1.64e-05    1.72e-05    1.72e-05   -3.66e-06    1.64e-05    3.36e-05    1.62e-05
VGS           1.941       1.949       1.922      -1.492       1.905       1.959       1.911
VDS           1.966       1.949       1.922      -2.069       3.975       4.059       2.573
VBS          -1.059      -1.059      -1.008       0.         -1.025       0.         -1.019
VTH           1.566       1.566       1.537      -0.882       1.534       0.876       1.539
VDSAT         0.242       0.247       0.246      -0.457       0.239       0.605       0.239
GM            8.79e-05    8.98e-05    8.95e-05    1.21e-05    8.88e-05    6.34e-05    8.75e-05
GDS           8.74e-07    9.00e-07    8.99e-07    6.87e-08    6.70e-07    2.29e-07    7.87e-07
GMB           4.65e-05    4.75e-05    4.81e-05    3.98e-06    4.74e-05    4.98e-05    4.69e-05
CBD           8.67e-15    8.69e-15    8.78e-15    1.01e-14    7.01e-15    7.67e-15    8.08e-15
CBS           1.26e-14    1.26e-14    1.28e-14    2.00e-14    1.27e-14    2.00e-14    1.28e-14
CGSOVL        2.84e-14    2.84e-14    2.84e-14    1.22e-14    2.84e-14    2.27e-14    2.84e-14
CGDOVL        2.84e-14    2.84e-14    2.84e-14    1.22e-14    2.84e-14    2.27e-14    2.84e-14
CGBOVL        1.72e-17    1.72e-17    1.72e-17    3.76e-17    1.72e-17    4.72e-17    1.72e-17
DERIVATIVES OF GATE (DQGDVX) AND BULK (DQBDVX) CHARGES
DQGDVGB       2.74e-13    2.74e-13    2.75e-13    2.84e-13    2.74e-13    6.18e-13    2.75e-13
DQGDVDB       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
DQGDVSB      -2.33e-13   -2.33e-13   -2.33e-13   -2.56e-13   -2.33e-13   -5.18e-13   -2.33e-13
DQBDVGB      -4.13e-14   -4.12e-14   -4.16e-14   -3.26e-14   -4.14e-14   -1.18e-13   -4.15e-14
DQBDVDB       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
DQBDVSB      -1.30e-13   -1.30e-13   -1.32e-13   -9.23e-14   -1.31e-13   -4.43e-13   -1.32e-13


            M5          M11         M12         M8          M9          M10         M14

MODEL       MP          MP          MN          MN          MP          MP          MP
ID           -2.79e-05   -1.62e-05    4.41e-05    1.65e-05   -1.65e-05   -1.65e-05   -2.00e-05
VGS          -1.408      -1.492       1.959       1.959      -1.667      -1.492      -1.492
VDS          -3.981      -1.408       6.019       1.959      -5.716      -2.325      -1.492
VBS           0.          0.          0.          0.          2.325       0.          0.
VTH          -0.856      -0.883       0.866       0.879      -1.350      -0.881      -0.863
VDSAT        -0.415      -0.456       0.613       0.602      -0.272      -0.457      -0.472
GM            1.02e-04    5.38e-05    8.26e-05    3.13e-05    1.04e-04    5.46e-05    6.39e-05
GDS           9.09e-07    3.51e-07    3.14e-07    1.56e-07    6.90e-07    2.97e-07    9.05e-07
GMB           3.13e-05    1.77e-05    6.40e-05    2.46e-05    1.53e-05    1.80e-05    1.96e-05
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CBD        7.73e-15  1.15e-14  6.46e-15  1.03e-14  5.66e-15  9.62e-15  1.13e-14
CBS        2.00e-14  2.00e-14  2.00e-14  2.00e-14  9.62e-15  2.00e-14  2.00e-14
CGSOVL     4.88e-14  5.49e-14  2.27e-14  1.14e-14  7.32e-14  5.49e-14  2.88e-14
CGDOVL     4.88e-14  5.49e-14  2.27e-14  1.14e-14  7.32e-14  5.49e-14  2.88e-14
CGBOVL     1.76e-17  3.76e-17  3.72e-17  4.72e-17  1.76e-17  3.76e-17  1.76e-17
DERIVATIVES OF GATE (DQGDVX) AND BULK (DQBDVX) CHARGES
DQGDVGB    5.37e-13  1.28e-12  4.86e-13  3.09e-13  7.69e-13  1.28e-12  3.17e-13
DQGDVDB    0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
DQGDVSB   -4.79e-13 -1.15e-12 -4.08e-13 -2.59e-13 -7.15e-13 -1.15e-12 -2.83e-13
DQBDVGB   -5.72e-14 -1.47e-13 -9.22e-14 -5.89e-14 -4.78e-14 -1.47e-13 -3.37e-14
DQBDVDB    0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
DQBDVSB   -1.64e-13 -4.16e-13 -3.46e-13 -2.22e-13 -1.14e-13 -4.15e-13 -9.77e-14


             M1.X1     M2.X1     M3.X1     M4.X1     M5.X1     M6.X1     M7.X1

MODEL      MN        MN        MN        MP        MP        MP        MN
ID         2.34e-06  1.83e-06  4.17e-06 -1.83e-06 -2.34e-06 -1.75e-05  4.00e-06
VGS           1.034     1.015     1.547    -1.566    -1.656    -1.566     1.547
VDS           3.359     3.448     4.985    -1.566    -1.656    -2.069     1.547
VBS          0.        0.        0.        0.        0.        0.        0.
VTH           0.870     0.870     0.867    -0.883    -0.882    -0.888     0.875
VDSAT         0.086     0.076     0.371    -0.513    -0.583    -0.508     0.366
GM         2.87e-05  2.53e-05  1.25e-05  5.39e-06  6.12e-06  5.22e-05  1.21e-05
GDS        7.12e-08  6.07e-08  3.99e-08  3.70e-08  4.55e-08  2.08e-07  6.48e-08
GMB        2.58e-05  2.28e-05  1.03e-05  1.75e-06  1.95e-06  1.73e-05  1.00e-05
CBD        8.31e-15  8.22e-15  7.02e-15  1.11e-14  1.09e-14  1.01e-14  1.12e-14
CBS        2.00e-14  2.00e-14  2.00e-14  2.00e-14  2.00e-14  2.00e-14  2.00e-14
CGSOVL     5.68e-14  5.68e-14  5.68e-15  4.88e-15  4.88e-15  7.32e-14  5.68e-15
CGDOVL     5.68e-14  5.68e-14  5.68e-15  4.88e-15  4.88e-15  7.32e-14  5.68e-15
CGBOVL     3.72e-17  3.72e-17  3.72e-17  3.76e-17  3.76e-17  5.76e-17  3.72e-17
DERIVATIVES OF GATE (DQGDVX) AND BULK (DQBDVX) CHARGES
DQGDVGB    1.24e-12  1.25e-12  1.23e-13  1.14e-13  1.13e-13  2.61e-12  1.23e-13
DQGDVDB    0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
DQGDVSB   -1.01e-12 -1.01e-12 -1.02e-13 -1.03e-13 -1.03e-13 -2.36e-12 -1.02e-13
DQBDVGB   -2.42e-13 -2.42e-13 -2.36e-14 -1.29e-14 -1.28e-14 -3.00e-13 -2.37e-14
DQBDVDB    0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
DQBDVSB   -9.29e-13 -9.30e-13 -8.92e-14 -3.67e-14 -3.63e-14 -8.53e-13 -8.97e-14
 *******03/24/86 ******** .SPICE 2G.6    3/15/83 ********18:37:20*****

BUFFER AMPLIFIER


****     AC ANALYSIS                          TEMPERATURE =   27.000 DEG C


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```
LEGEND:

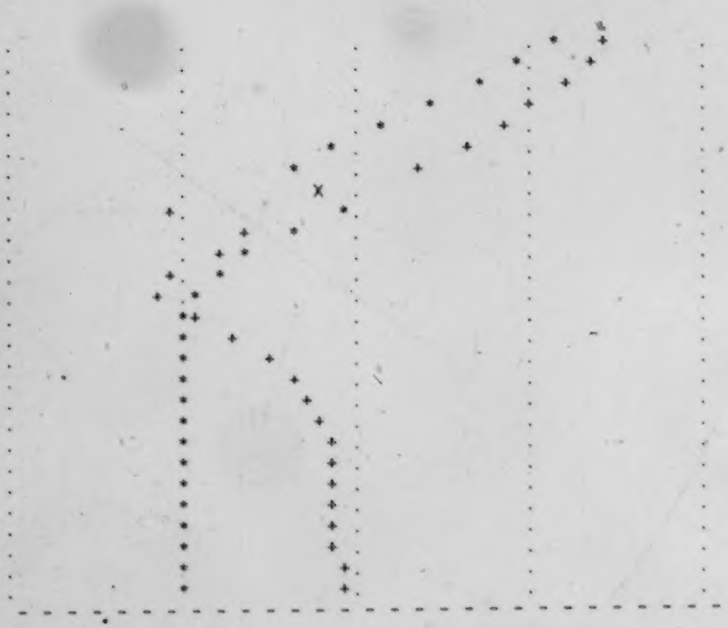
*: VDB(13)
+: VDB(6)

    FREQ       VDB(13)

*)------------- -1.500d+01    -1.000d+01    -5.000d+00     0.000d+00 5.000d+00
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

+)------------- -3.000d+01    -2.000d+01    -1.000d+01     0.000d+00 1.000d+01
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
1.000d+03 -2.055d-02 .             .             .             *    +        .
1.259d+03 -2.055d-02 .             .             .             *    +        .
1.585d+03 -2.055d-02 .             .             .             *    +        .
1.995d+03 -2.055d-02 .             .             .             *    +        .
2.512d+03 -2.055d-02 .             .             .             *    +        .
3.162d+03 -2.055d-02 .             .             .             *    +        .
3.981d+03 -2.054d-02 .             .             .             *    +        .
5.012d+03 -2.053d-02 .             .             .             *    +        .
6.310d+03 -2.052d-02 .             .             .             *    +        .
7.943d+03 -2.050d-02 .             .             .             *    +        .
1.000d+04 -2.047d-02 .             .             .             *    +        .
1.259d+04 -2.043d-02 .             .             .             *    +        .
1.585d+04 -2.036d-02 .             .             .             *    +        .
1.995d+04 -2.024d-02 .             .             .             *    +        .
2.512d+04 -2.006d-02 .             .             .             *    +        .
3.162d+04 -1.977d-02 .             .             .             *    +        .
3.981d+04 -1.932d-02 .             .             .             *    +        .
5.012d+04 -1.860d-02 .             .             .             *    +        .
6.310d+04 -1.746d-02 .             .             .             *    +        .
7.943d+04 -1.565d-02 .             .             .             *    +        .
1.000d+05 -1.279d-02 .             .             .             *    +        .
1.259d+05 -8.266d-03 .             .             .             *    +        .
1.585d+05 -1.123d-03 .             .             .             *    +        .
1.995d+05  1.013d-02 .             .             .             *    +        .
2.512d+05  2.781d-02 .             .             .             *    +        .
3.162d+05  5.542d-02 .             .             .             *    +        .
3.981d+05  9.818d-02 .             .             .             *    +        .
5.012d+05  1.634d-01 .             .             .             *     +       .
6.310d+05  2.608d-01 .             .             .             .*    +       .
7.943d+05  4.003d-01 .             .             .             .*    +       .
1.000d+06  5.866d-01 .             .             .             . *   +       .
1.259d+06  8.036d-01 .             .             .             . *   +       .
1.585d+06  9.845d-01 .             .             .             .  *   +      .
1.995d+06  9.821d-01 .             .             .             .  *  +       .
```

```
2.512d+06  6.001d-01
3.162d+06 -2.614d-01
3.981d+06 -1.506d+00
5.012d+06 -2.951d+00
6.310d+06 -4.457d+00
7.943d+06 -5.891d+00
1.000d+07 -6.823d+00
1.259d+07 -6.055d+00
1.585d+07 -5.474d+00
1.995d+07 -6.923d+00
2.512d+07 -8.207d+00
3.162d+07 -9.050d+00
3.981d+07 -9.572d+00
5.012d+07 -9.876d+00
6.310d+07 -1.004d+01
7.943d+07 -1.010d+01
1.000d+08 -1.012d+01
1.259d+08 -1.012d+01
1.585d+08 -1.010d+01
1.995d+08 -1.009d+01
2.512d+08 -1.007d+01
3.162d+08 -1.006d+01
3.981d+08 -1.006d+01
5.012d+08 -1.005d+01
6.310d+08 -1.005d+01
7.943d+08 -1.005d+01
1.000d+09 -1.005d+01
```



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*******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****

BUFFER AMPLIFIER

****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

*************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    1.0000    (  2)   -0.9407    (  3)    1.0253    (  5)    1.0084

(  6)    2.9307    (  7)    5.0000    (  8)    3.5078    (  9)    2.6755
( 10)   -3.0408    ( 11)   -5.0000    ( 12)    3.5923    ( 13)    1.0193
( 14)   -2.0000    ( 15)    0.        ( 30)    2.9307    ( 31)    3.3445
( 32)   -0.0148    ( 33)    3.4336    ( 34)   -3.4530


    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VIN        0.000d+00
    VBOG       1.752d-05
    VSUB1      1.130d-11
    VSUB2      2.021d-11
    VDD       -1.225d-04
    VSS       -1.025d-04

    TOTAL POWER DISSIPATION   1.03d-03  WATTS
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****

BUFFER AMPLIFIER

****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

***********************************************************************



**** MOSFETS


              M1         M2         M3         M6         M7         M13        M4
```
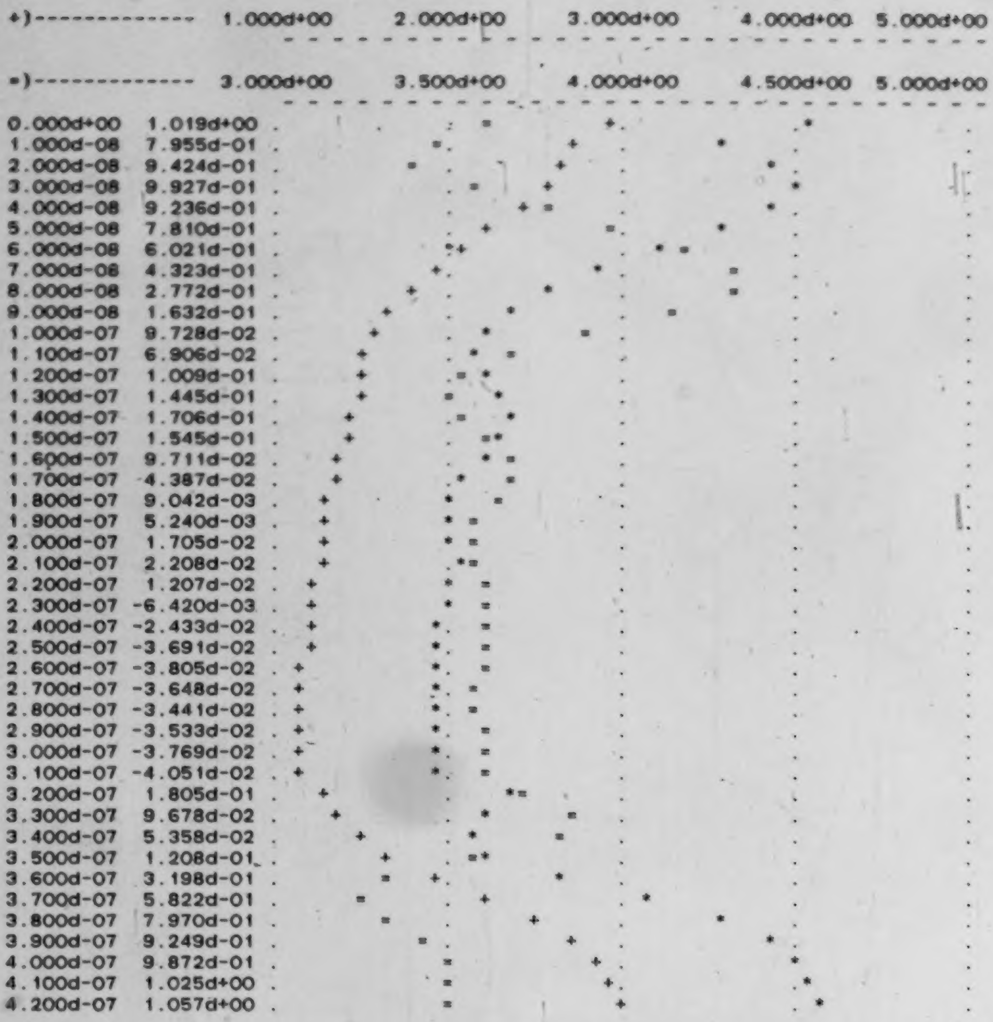

```
MODEL      MN         MN         MN         MP         MN         MN         MN
ID         1.64e-05   1.72e-05   1.72e-05  -3.66e-06   1.64e-05   3.36e-05   1.62e-05
VGS           1.941      1.949      1.922     -1.492      1.905      1.959      1.911
VDS           1.966      1.949      1.922     -2.069      3.975      4.059      2.573
VBS          -1.059     -1.059     -1.008      0.        -1.025      0.        -1.019


             M5         M11        M12        M8         M9         M10        M14

MODEL      MP         MP         MN         MN         MP         MP         MP
ID        -2.79e-05  -1.62e-05   4.41e-05   1.65e-05  -1.65e-05  -1.65e-05  -2.00e-05
VGS          -1.408     -1.492      1.959      1.959     -1.667     -1.492     -1.492
VDS          -3.981     -1.408      6.019      1.959     -5.716     -2.325     -1.492
VBS           0.         0.         0.         0.         2.325      0.         0.


             M1.X1      M2.X1      M3.X1      M4.X1      M5.X1      M6.X1      M7.X1

MODEL      MN         MN         MN         MP         MP         MP         MN
ID         2.34e-06   1.83e-06   4.17e-06  -1.83e-06  -2.34e-06  -1.75e-05   4.00e-06
VGS           1.034      1.015      1.547     -1.566     -1.656     -1.566      1.547
VDS           3.359      3.448      4.985     -1.566     -1.656     -2.069      1.547
VBS           0.         0.         0.         0.         0.         0.         0.
 *******03/24/86 ********  SPICE 2G.6    3/15/83 ********18:37:20*****

BUFFER AMPLIFIER

****     TRANSIENT ANALYSIS                   TEMPERATURE =   27.000 DEG C

******************************************************************************


LEGEND:

*: V(13)
+: V(6)
=: V(12)

   TIME        V(13)

*)------------- -5.000d-01     0.000d+00     5.000d-01     1.000d+00  1.500d+00
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```



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=)-------------  3.000d+00    3.500d+00    4.000d+00    4.500d+00  5.000d+00

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5.000d-08   7.810d-01
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9.000d-08   1.632d-01
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1.100d-07   6.906d-02
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5.000d-07   1.089d+00
5.100d-07   1.082d+00
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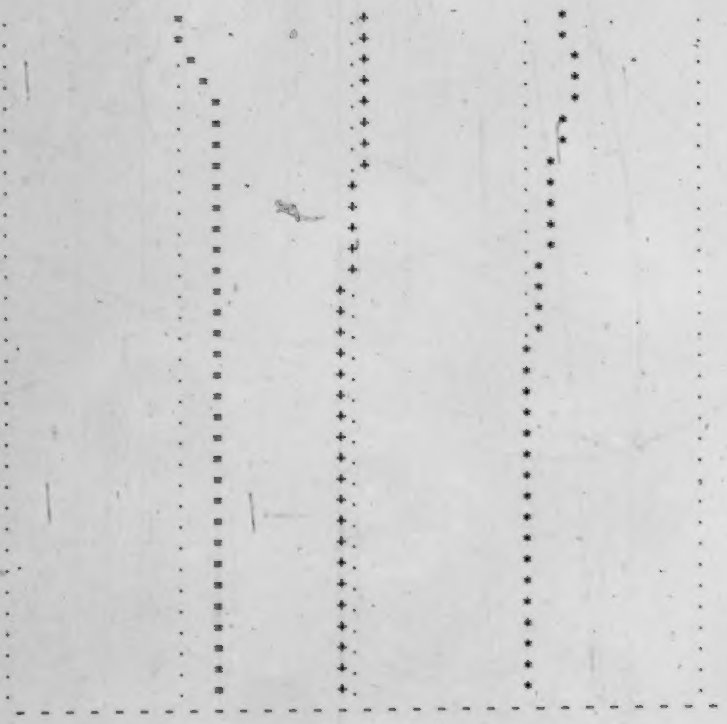

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JOB CONCLUDED

 TOTAL JOB TIME          257.92
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